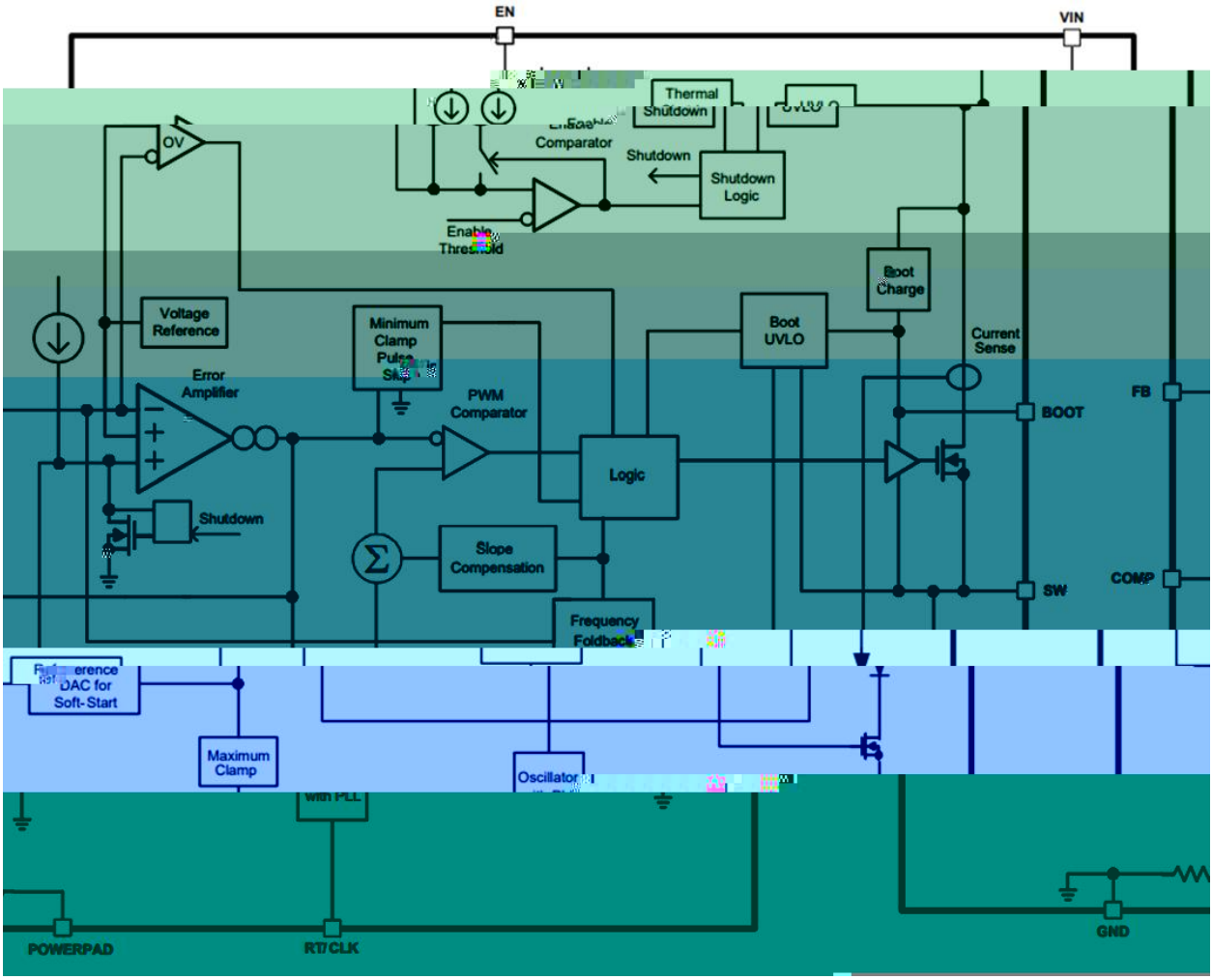
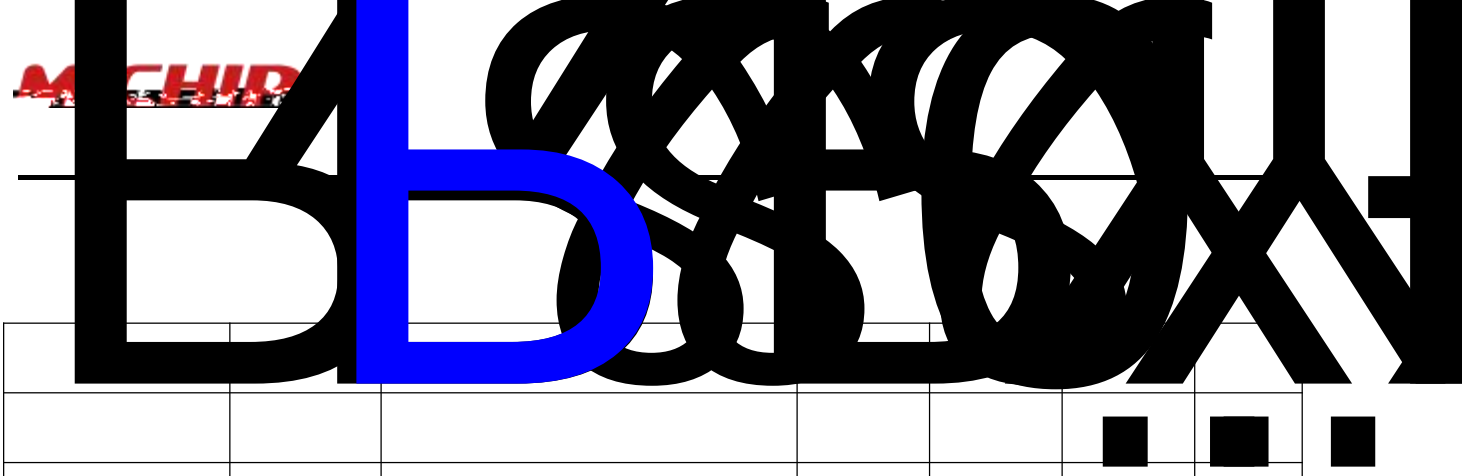
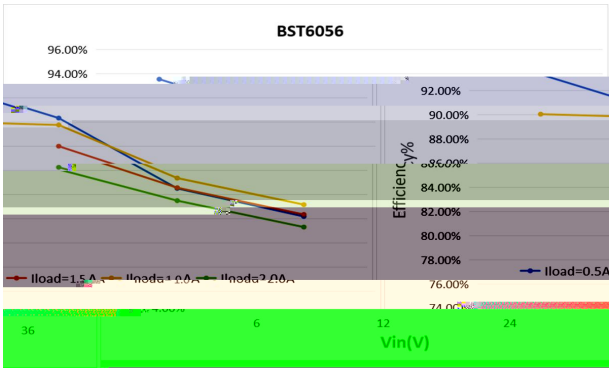

ESOP8
BOOT
VIN
1
8
SW
GND

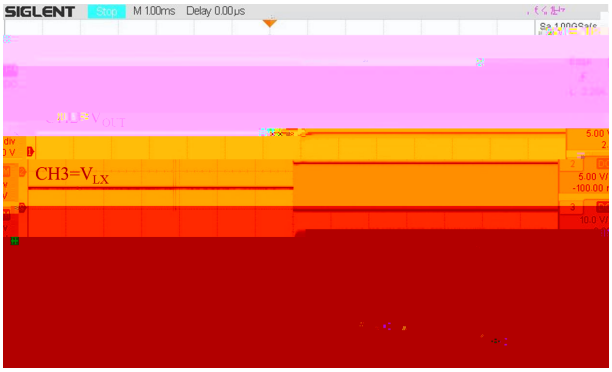

EN
VIN
Thermal Shutdown
UVLO
Comparator
Shutdown
Shutdown Logic
Enable Threshold
OV
Boot Charge
Voltage Reference
Minimum Clamp Pulse Skip
Boot UVLO
Current Sense
Error Amplifier
PWM Comparator
FB
BOOT
Logic
Shutdown
Slope Compensation
SW
COMP
Frequency Foldback
Reference DAC for Soft-Start
Maximum Clamp
Oscillator
with PLL
POWERPAD
RT/CLK
GND

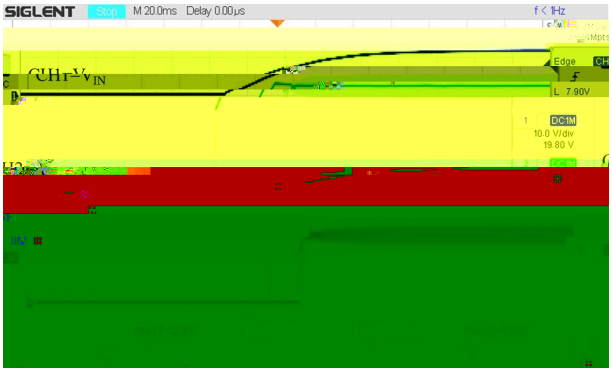


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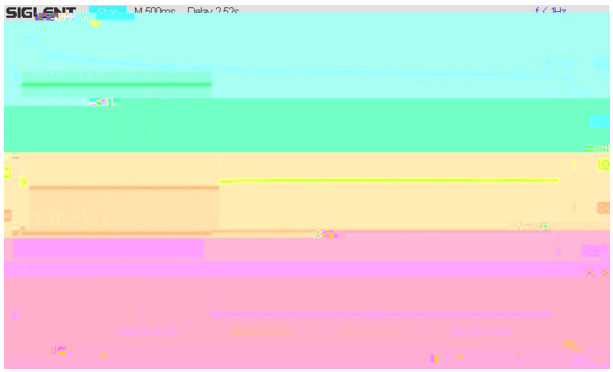

BST6056
96.00%
94.00%
92.00%
90.00%
88.00%
84.00%
82.00%
80.00%
78.00%
76.00%
Efficiency%
Iload=0.5A
36
6
12
24
Vin(V)

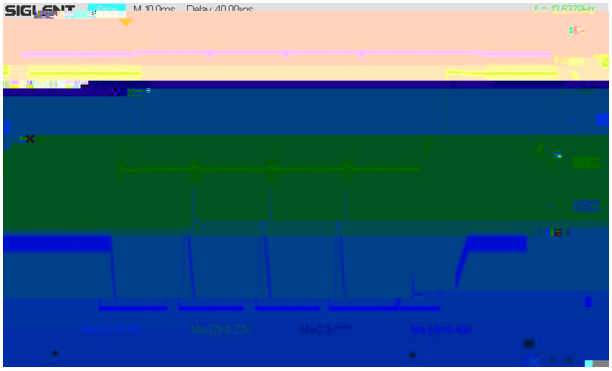

SIGLENT
Stop
M 1.00ms
Delay 0.00µs
CH3=V_LX

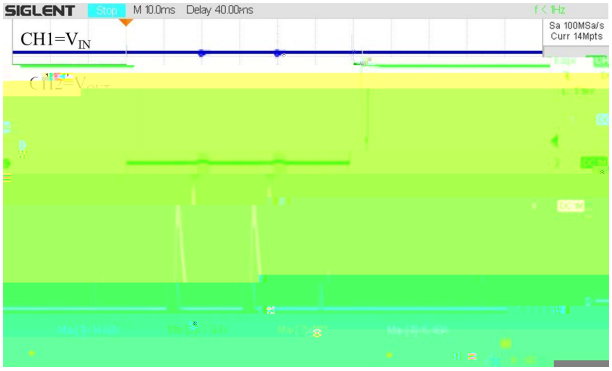

SIGLENT
Stop
M 20.0ms
Delay 0.00µs
CH1=V_IN
Edge
L 7.90V
DC1M
10.0 V/div
19.80 V

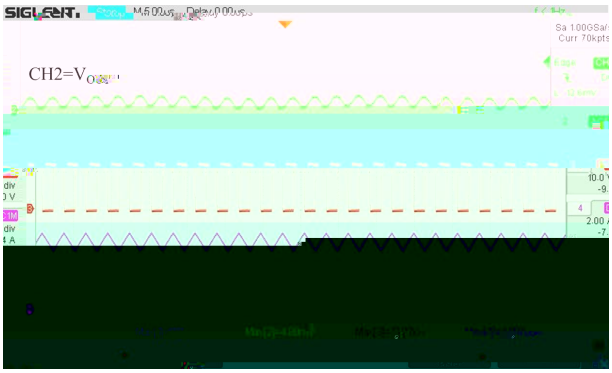

SIGLENT
Stop
M 20.0ms
Delay 0.00µs
CH1=V_IN
Sa 50.0MSa/s
Edge
DC


SIGLENT
Stop
M 20.0ms
Delay 0.00µs


SIGLENT

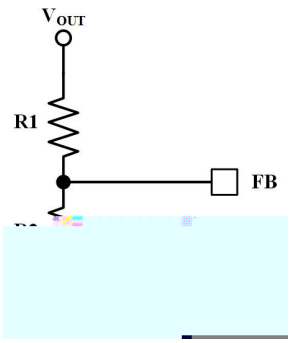



SIGLENT
Stop
M 10.0ms Delay 40.00ms
Sa 100MSa/s
Curr 14Mpts
CH1=V_{IN}


CH2=V_{OUT}


SIGLENT
Stop
M 500ms Delay 10.00ms
Sa 200kSa/s
Curr 1.4Mpts
CH1=V_{OUT}
CH2=V_{IN}
ΔV= -2.00V
Y2 = 58.0V
Y1 = 60.0V
1.00 V/div
-2.00 V
2.00 V/div
-57.00 V
Max{1}=5.16V
Max{2}=60.08V
Min{2}=57.68V
类型
屏幕
按下

$$R_1 = R_2 \frac{V_{out} - 0.8V}{0.8V}$$



$$I_{CIN_RMS} = I_{OUT} * \sqrt{D(1-D)}$$

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN_MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

$$I_{SAT_MIN} > I_{OUT}$$

, õ #2 $ 10 Qb 0 `