S6J3360 Series
S6J3370 Series

32-bit ARM® Cortex®-R5F Traveo

Table of Contents

1. Features 4
1.1 Function List 4
1.2 Optional Function 7
1.2.1 Basic Option 7
1.2.2 ID 8
2. Handling Precauti

Function	S6J33xxJxx 176-pin	S6J33xxHxx 144-pin	S6J33xxGxx 120-pin	S6J33xxFxx 100-pin	Remarks

1.2 Optional Function

1.2.1 Basic Option

The following figure shows the optional functions and the part number relations of the series.

◆Basic Option

S 6 J 3 3 0 0 H A A S V 2 0 x x x

Ordering options 3 digit

Packing

Package

Reliability

Revision : Revision version

Option :

[1] VCC5 ≧ VCC53_1/VCC53_2

Pin count

Memory size

[2] Including Back-up RAM area. Back-up RAM size is16+8KB.

Function :

Note:

- *This table only shows the relation between the optional function and the part numbers; that is, all products are not necessarily available for orders. See the order number on the datasheet and confirm product availability.*
- *Relationship of Package option and Pin count option is as follows*

○ Support — Not support.

1.2.2 ID

ID is specified for each Memory size digit, Option digit and revision.

Memory size	Option	Revision	Chip ID	JTAG ID	SHE Module ID (SHE_MID) *
C	S	A	0x10160100	0x002505CF	0x000F_0300
	T			0x002515CF	
	U			0x002525CF	
	V			0x002535CF	
	A		0x10168100	0x002505CF	
	E			0x002515CF	
	C			0x002525CF	
	G			0x002535CF	
B	S		0x10160100	0x002545CF	
	T			0x002555CF	
	U			0x002565CF	
	V			0x002575CF	
	A		0x10168100	0x002545CF	
	E			0x002555CF	
	C			0x002565CF	
	G			0x002575CF	

A

2. Handling Precautions

3. Handling Devices

Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC5 or lower than VSS; or the voltage applied between a VCC5 pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC5, AVRH5) and analog inputs do not exceed the digital power supply (VCC5) at the analog ke

PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that AVCC5 = AVRH5 = VCC5, and AVSS = VSS.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC5) before the application of the power supplies (AVCC5, AVRH5) and analog inputs (ADC0_AN0 to ADC0_AN47) of an A/D converter. At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC5). Perform these power-on and power-off operations without AVRH5 exceeding AVCC5. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC5. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

C-Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (refer to the pin assignment) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest datasheet.

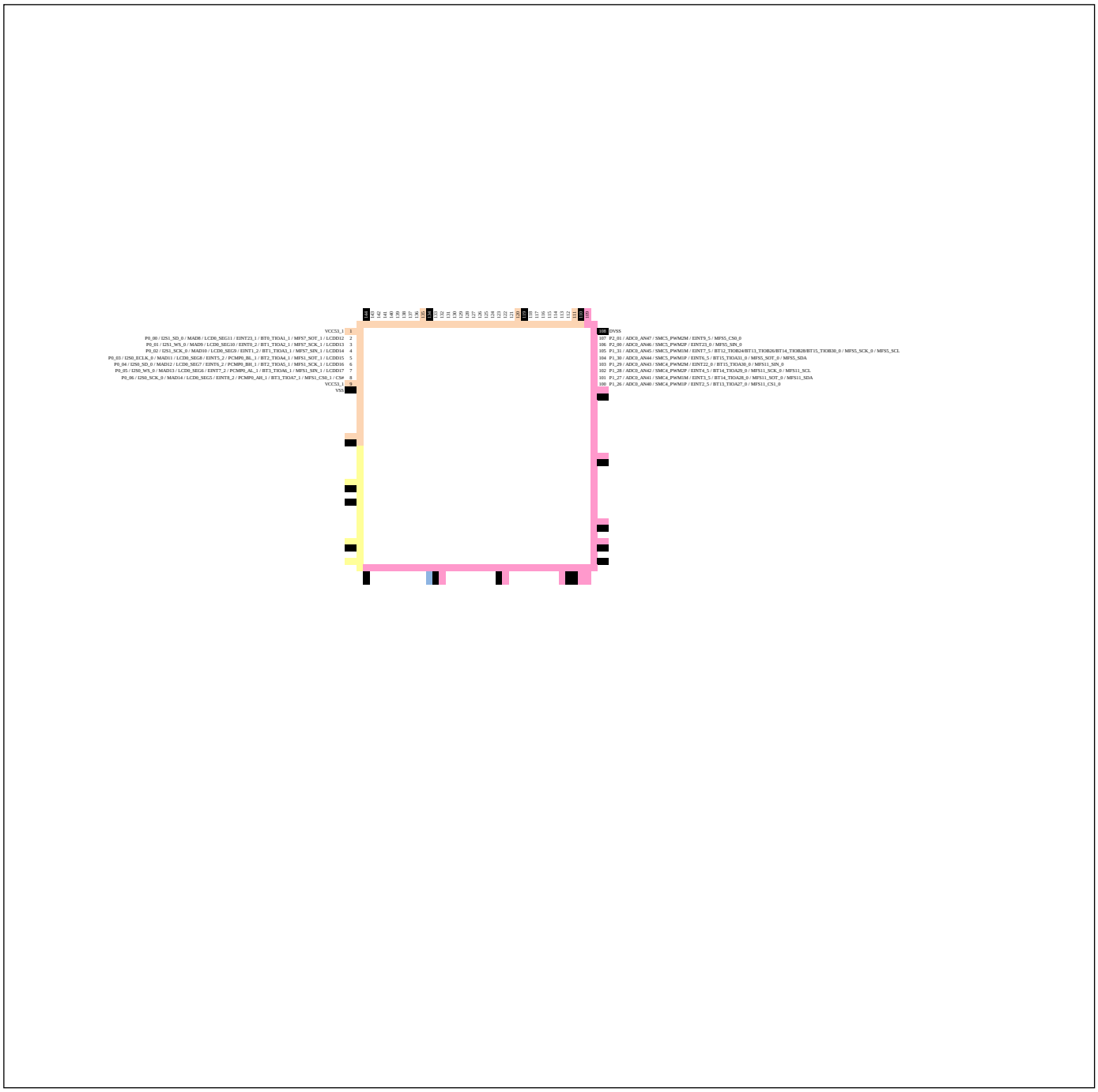
Writing to a Register Containing a Status Flag

When you write to a register containing a status flag (such as an interrupt request flag) to control a function, take care not to accidentally clear the status flag. Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value. Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions only have 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into consideration for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

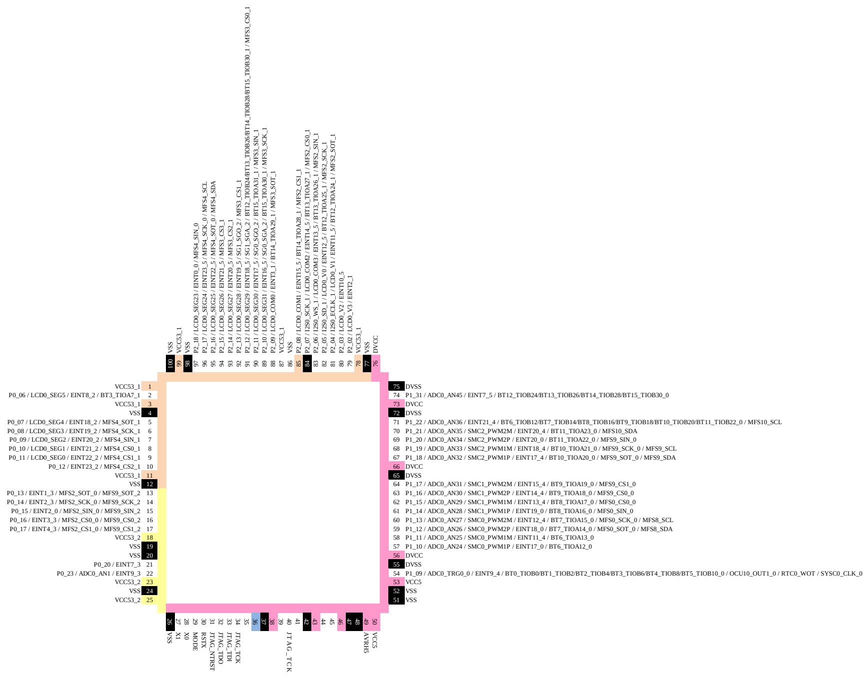
4.2 LQFP/TEQFP-144 Pin Assignment

Figure 4-2: LQFP/TEQFP-144



4.4 LQFP/TEQFP-100 Pin Assignment

Figure 4-4: LQFP/TEQFP-100



5. Pin Descriptions

5.1 Pin descriptions

5.1.1 LQFP176/ TEQFP176

Table 5-1-1: Pin Descriptions of LQFP176/ TEQFP176of

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
1	VCC53_1	-	+3.3 V/ +5.0 V selection power supply pin (1)
2	P0_00	P	GPIO port
	I2S1_SD_0		I2S ch.1 serial data I/O pin_0
	MAD8		External BUS Interface address output pin
	LCD0_SEG11		LCD controller segment output pin
	EINT23_1		External interrupt ch.23 input pin_1
	BT0_TIOA1_1		Base timer0 ch.1 TIOA output pin_1

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
14	P3_03	A	GPIO port
	MAD18		External BUS Interface address output pin
	EINT11_2		External interrupt ch.11 input pin_2
	BT5_TIOA11_1		Base timer5 ch.11 TIOA output pin_1

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
	P0_11		GPIO port
	MCSX2		External BUS Interface chip select output pin
	LCD0_SEG0		
23		P	

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
34	P0_18	M	GPIO port
	DDRHSSPI0_SCLK		DDR HSSPI serial clock output pin
	EINT5_3		External interrupt ch.5 input pin_3
	MFS2_CS2_0		Multi-function serial ch.2 serial chip select 2 output pin_0
35	VSS	-	GND
36	P0_19	M	GPIO port
	DDRHSSPI0_SDATA0		DDR HSSPI serial data I/O pin
	EINT6_3		External interrupt ch.6 input pin_3
	MFS2_CS3_0		Multi-function serial ch.2 serial chip select 3 output pin_0
	MFS8_SOT_2		Multi-function serial ch.8 serial data output pin_2
37	P0_20	M	GPIO port
	DDRHSSPI0_SDATA2		DDR HSSPI serial data I/O pin
	EINT7_3		External interrupt ch.7 input pin_3
	MFS3_SOT_0		Multi-function serial ch.3 serial data output pin_0
	MFS8_SCK_2		Multi-function serial ch.8 clock I/O pin_2
38	P0_21	M	GPIO port
	DDRHSSPI0_SDATA1		DDR HSSPI serial data I/O pin
	EINT8_3		External interrupt ch.8 input pin_3
	MFS3_SCK_0		Multi-function serial ch.3 clock I/O pin_0
	MFS8_SIN_2		Multi-function serial ch.8 serial data input pin_2
39	P0_22	M	GPIO port
	DDRHSSPI0_SSEL		DDR HSSPI select output pin
	ADC0_AN0		ADC ch.0 analog input pin
	EINT3_0		External interrupt ch.3 input pin_0
	MFS3_SIN_0		Multi-function serial ch.3 serial data input pin_0
	MFS8_CS0_2		Multi-function serial ch.8 serial chip select 0 I/O pin_2
40	P0_23	M	GPIO port
	DDRHSSPI0_SDATA3		DDR HSSPI serial data I/O pin
	ADC0_AN1		ADC ch.1 analog input pin
	EINT9_3		External interrupt ch.9 input pin_3
	MFS3_CS0_0		Multi-function serial ch.3 serial chip select 0 I/O pin_0
41	VCC53_2	-	+3.3 V/ +5.0 V selection power supply pin (2)
42	VSS	-	GND
43	P0_24	M	GPIO port
	ADC0_AN2		ADC ch.2 analog input pin
	EINT10_3		External interrupt ch.10 input pin_3
	MFS3_CS1_0		Multi-function serial ch.3 serial chip select 1 output pin_0

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
62	P3_12	A	GPIO port
	ADC0_AN4		ADC ch.4 analog input pin
	EINT21_1		External interrupt ch.21 input pin_1
	SG2_SGA_1		Sound generator ch.2 SGA output pin_1
	BT8_TIOA16_1		Base timer8 ch.16 TIOA output pin_1
	OCU2_OUT0_1		Output compare2 ch.0 output pin_1
	ICU2_IN0_1		Input capture2 ch.0 input pin_1
	RLT16_TIN_1		Reload timer ch.16 event input pin_1
	CAN1_TX_1		CAN ch.1 transmission data output pin_1
	MFS10_SCK_1		Multi-function serial ch.10 clock I/O pin_1
	TRACE_CLK_1		Trace clock output pin_1
63	P3_13	A	GPIO port
	ADC0_AN5		ADC ch.5 analog input pin
	EINT18_3		External interrupt ch.18 input pin_3
	SG2_SGO_1		Sound generator ch.2 SGO output pin_1
	BT8_TIOA17_1		Base timer8 ch.17 TIOA output pin_1
	OCU2_OUT1_1		Output compare2 ch.1 output pin_1
	ICU2_IN1_1		Input capture2 ch.1 input pin_0
	RLT16_TOT_1		Reload timer ch.16 output pin_1
	MFS10_SIN_1		Multi-function serial ch.10 serial data input pin_1
	TRACE_CTL_1		Trace control output pin_1
64	P0_25	A	GPIO port
	ADC0_AN6		ADC ch.6 analog input pin
	EINT4_0		External interrupt ch.4 input pin_0
	PCMP0_BL_0		PCM_PWM ch.0 BL output pin_0
	BT0_TIOA0_0		Base timer0 ch.0 TIOA output pin_0
	OCU0_OUT0_0		Output compare0 ch.0 output pin_0
	ICU0_IN0_0		Input capture0 ch.0 input pin_0
	QPRC8_AIN		Quadrature Position and Revolution Counter ch.8 AIN input pin
	RLT0_TIN_0		Reload timer ch.0 event input pin_0
	FRT0/1/2/3_TEXT		Free-run timer ch.0/1/2/3 clock input pin
	CAN0_RX_0		CAN ch.0 reception data input pin_0
	MFS8_SOT_0		Multi-function serial ch.8 serial data output pin_0
	MFS0_SDA		I2C ch.0 serial data I/O pin
	PWU_AN0		Partial wakeup ADC analog 0 input pin
65	P0_26	A	GPIO port
	ADC0_AN7		ADC ch.7 analog input pin
	EINT5_0		External interrupt ch.5 input pin_0
	PCMP0_BH_0		PCM_PWM ch.0 BH output pin_0
	BT0_TIOA1_0		Base timer0 ch.1 TIOA output pin_0
	OCU0_OUT1_0		Output compare0 ch.1 output pin_0
	ICU0_IN1_0		Input capture0 ch.1 input pin_0
	QPRC8_BIN		Quadrature Position and Revolution Counter ch.8 BIN input pin
	RLT0_TOT_0		Reload timer ch.0 output pin_0
	FRT4/8/9/10_TEXT		Free-run timer ch.4/8/9/10 clock input pin
	CAN0_TX_0		CAN ch.0 transmission data output pin_0
	MFS8_SCK_0		Multi-function serial ch.8 clock I/O pin_0
	MFS0_SCL		I2C ch.0 clock I/O pin
	PWU_AN1		Partial wakeup ADC analog 1 input pin

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
	P0_27		GPIO port
	ADC0_AN8		ADC ch.8 analog input pin
	EINT6_0		External interrupt ch.6 input pin_0
66		A	

P97t TJET1 0 0 1 548.76 731.76

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
77	P1_03	C	GPIO port
	ADC0_AN14		ADC ch.14 analog input pin
	EINT19_3		External interrupt ch.19 input pin_3
	PCMP1_AH_0		PCM_PWM ch.1 AH output pin_0
	SG2_SGO_0		Sound generator ch.2 SGO output pin_0
	BT3_TIOA7_0		Base timer3 ch.7 TIOA output pin_0
	OCU2_OUT1_0		Output compare2 ch.1 output pin_0
	ICU8_IN1_0		Input capture8 ch.1 input pin_0
	MFS6_SCK_0		Multi-function serial ch.6 clock I/O pin_0
	MFS6_SCL		I2C ch.6 clock I/O pin
	TRACE3_0		Trace data 3 output pin_0
	PWU_AN5		Partial wakeup ADC analog 5 input pin
78	P1_04	A	GPIO port
	ADC0_AN15		ADC ch.15 analog input pin
	EINT13_0		External interrupt ch.13 input pin_0
	SG3_SGA_0		Sound generator ch.3 SGA output pin_0
	BT9_TIOA19_1		Base timer9 ch.19 TIOA output pin_1
	OCU8_OUT1_1		Output compare8 ch.1 output pin_1
	ICU8_IN1_1		

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
91	P3_17	A	GPIO port
	EINT17_1		External interrupt ch.17 input pin_1
	BT11_TIOA23_1		Base timer11 ch.23 TIOA output pin_1
	OCU10_OUT1_1		Output compare10 ch.1 output pin_1
	ICU10_IN1_1		Input capture10 ch.1 input pin_1
	CAN3_RX_1		CAN ch.3 reception data input pin_1
	MFS9_SCK_1		Multi-function serial ch.9 clock I/O pin_1
92	P3_18	A	GPIO port
	EINT2_4		External interrupt ch.2 input pin_4
	BT10_TIOA21_1		Base timer10 ch.21 TIOA output pin_1
	RLT3_TIN_1		Reload timer ch.3 event input pin_1

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
	P1_09		GPIO port
	ADC0_TRG0_0		ADC external trigger ch.0 input pin_0
	EINT9_4		External interrupt ch.9 input pin_4
101	BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_0	A	

LQFP176/ TEQFP176

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
119	P1_23	O	GPIO port
	ADC0_AN37		ADC ch.37 analog input pin
	SMC3_PWM1M		Stepper Motor Controller ch.3 PWM1M output pin
	EINT21_0		External interrupt ch.21 input pin_0
	BT12_TIOA24_0		Base timer12 ch.24 TIOA output pin_0
	MFS10_SIN_0		Multi-function serial ch.10 serial data input pin_0
120	P1_24	O	GPIO port
	ADC0_AN38		ADC ch.38 analog input pin
	SMC3_PWM2P		Stepper Motor Controller ch.3 PWM2P output pin
			ch.22 input pin_4
			5 TIOA output pin_0
			al ch.10 serial chip select 0 I/O pin_0
			input pin
			ntroller ch.3 PWM2M output pin
			ch.0 input pin_5
			6 TIOA output pin_0
			al ch.11 serial chip select 0 I/O pin_0
			port GND pin
			port power supply pin
			input pin
			ntroller ch.4 PWM1P output pin
			ch.2 input pin_5

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
128	P1_30 ADC0_AN44 SMC5_PWM1P	O	GPIO port ADC ch.44 analog input pin

LQFP176/ TEQFP176			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
160	P2_18	P	GPIO port
	MDATA4		External BUS Interface data I/O pin
	LCD0_SEG23		LCD controller segment output pin
	EINT0_0		External interrupt ch.0 input pin_0
	MFS4_SIN_0		Multi-function serial ch.4 serial data input pin_0
	LCDD3		LCD BUS interface data I/O pin
161	P2_19	P	GPIO port
	MDATA5		External BUS Interface data I/O pin
	LCD0_SEG22		

5.1.2 LQFP144/ TEQFP144

Table 5-1-2: Pin Descriptions of LQFP144/ TEQFP144

LQFP144/ TEQFP144		
Pin No.	**Pin Name**	**I/O**

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
	P0_11		GPIO port
15		P	

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
28	P0_19	M	GPIO port
	DDRHSSPI0_SDATA0		DDR HSSPI serial data I/O pin
	EINT6_3		External interrupt ch.6 input pin_3
	MFS2_CS3_0		Multi-function serial ch.2 serial chip select 3 output pin_0
	MFS8_SOT_2		Multi-function serial ch.8 serial data output pin_2
29	P0_20	M	GPIO port
	DDRHSSPI0_SDATA2		DDR HSSPI serial data I/O pin
	EINT7_3		External interrupt ch.7 input pin_3
	MFS3_SOT_0		Multi-function serial ch.3 serial data output pin_0
	MFS8_SCK_2		Multi-function serial ch.8 clock I/O pin_2
30	P0_21	M	GPIO port
	DDRHSSPI0_SDATA1		DDR HSSPI serial data I/O pin
	EINT8_3		External interrupt ch.8 input pin_3
	MFS3_SCK_0		Multi-function serial ch.3 clock I/O pin_0
	MFS8_SIN_2		Multi-function serial ch.8 serial data input pin_2
31	[redacted]	M	GPIO port
	DDRHSSPI0_SSEL		DDR HSSPI select output pin
	ADC0_AN0		ADC ch.0 analoN 155.4239.5 459u61 4499447.44 t n

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
50	P0_25	A	GPIO port
	ADC0_AN6		ADC ch.6 analog input pin
	EINT4_0		External interrupt ch.4 input pin_0
	PCMP0_BL_0		PCM_PWM ch.0 BL output pin_0
	BT0_TIOA0_0		Base timer0 ch.0 TIOA output pin_0
	OCU0_OUT0_0		Output compare0 ch.0 output pin_0
	ICU0_IN0_0		Input capture0 ch.0 input pin_0
	QPRC8_AIN		Quadrature Position and Revolution Counter ch.8 AIN input pin
	RLT0_TIN_0		Reload timer ch.0 event input pin_0
	FRT0/1/2/3_TEXT		Free-run timer ch.0/1/2/3 clock input pin
	CAN0_RX_0		CAN ch.0 reception data input pin_0
	MFS8_SOT_0		Multi-function serial ch.8 serial data output pin_0
	MFS0_SDA		I2C ch.0 serial data I/O pin

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
53	P0_28	A	GPIO port
	ADC0_AN9		ADC ch.9 analog input pin
	EINT7_0		External interrupt ch.7 input pin_0
	PCMP0_AH_0		PCM_PWM ch.0 AH output pin_0
	SG0_SGO_0		Sound generator ch.0 SGO output pin_0
	BT1_TIOA3_0		Base timer1 ch.3 TIOA output pin_0
	ICU1_IN1_0		Input capture1 ch.1 input pin_0
	QPRC9_AIN		Quadrature Position and Revolution Counter ch.9 AIN input pin
	RLT1_TOT_0		Reload timer ch.1 output pin_0
	CAN1_TX_0		CAN ch.1 transmission data output pin_0
	MFS8_CS0_0		Multi-function serial ch.8 serial chip select 0 I/O pin_0
	PWUTRG_0		Partial wakeup trigger output pin_0
54	P0_29	A	GPIO port
	ADC0_AN10		ADC ch.10 analog input pin
	EINT12_1		External interrupt ch.12 input pin_1
	BT9_TIOA18_1		Base timer9 ch.18 TIOA output pin_1
	OCU8_OUT0_1		Output compare8 ch.0 output pin_1
	ICU8_IN0_1		Input capture8 ch.0 input pin_1

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
60	P1_00	A	GPIO port
	ADC0_AN11		ADC ch.11 analog input pin
	EINT10_0		External interrupt ch.10 input pin_0
	PCMP1_BL_0		PCM_PWM ch.1 BL output pin_0
	SG1_SGA_0		Sound generator ch.1 SGA output pin_0
	BT2_TIOA4_0		Base timer2 ch.4 TIOA output pin_0
	OCU1_OUT0_0		Output compare1 ch.0 output pin_0
	ICU2_IN0_0		Input capture2 ch.0 input pin_0
	QPRC9_BIN		Quadrature Position and Revolution Counter ch.9 BIN input pin
	RLT16_TIN_0		Reload timer ch.16 event input pin_0
	CAN2_RX_0		CAN ch.2 reception data input pin_0
	IND0_OUT_0		Indicator PWM output pin_0
	TRACE0_0		Trace data 0 output pin_0
61	P1_01	A	GPIO port
	ADC0_AN12		ADC ch.12 analog input pin
	EINT11_0		External interrupt ch.11 input pin_0
	PCMP1_BH_0		PCM_PWM ch.1 BH output pin_0
	SG1_SGO_0		Sound generator ch.1 SGO output pin_0
	BT2_TIOA5_0		Base timer2 ch.5 TIOA output pin_0
	OCU1_OUT1_0		Output compare1 ch.1 output pin_0
	ICU2_IN1_0		Input capture2 ch.1 input pin_0
	QPRC9_ZIN		Quadrature Position and Revolution Counter ch.9 ZIN input pin
	RLT16_TOT_0		Reload timer ch.16 output pin_0
	CAN2_TX_0		CAN ch.2 transmission data output pin_0
	TRACE1_0		Trace data 1 output pin_0
	PWU_AN3		Partial wakeup ADC analog 3 input pin
62	P1_02	C	GPIO port
	ADC0_AN13		ADC ch.13 analog input pin
	EINT12_0		External interrupt ch.12 input pin_0
	PCMP1_AL_0		PCM_PWM ch.1 AL output pin_0
	SG2_SGA_0		Sound generator ch.2 SGA output pin_0
	BT3_TIOA6_0		Base timer3 ch.6 TIOA output pin_0
	OCU2_OUT0_0		Output compare2 ch.0 output pin_0
	ICU8_IN0_0		Input capture8 ch.0 input pin_0
	MFS6_SOT_0		Multi-function serial ch.6 serial data output pin_0
	MFS6_SDA		I2C ch.6 serial data I/O pin
	TRACE2_0		Trace data 2 output pin_0
	PWU_AN4		Partial wakeup ADC analog 4 input pin
	P1_03		GPIO port
	ADC0_AN14		ADC ch.14 analog input pin
	EINT19_3		External interrupt ch.19 input pin_3
	PCMP1_AH_0	C	PCM_PWM ch.1 AH output pin_0

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
64	P1_04	A	GPIO port
	ADC0_AN15		ADC ch.15 analog input pin
	EINT13_0		External interrupt ch.13 input pin_0
	SG3_SGA_0		Sound generator ch.3 SGA output pin_0
	BT9_TIOA19_1		Base timer9 ch.19 TIOA output pin_1
	OCU8_OUT1_1		Output compare8 ch.1 output pin_1
	ICU8_IN1_1		Input capture8 ch.1 input pin_1
	RLT17_TOT_1		Reload timer ch.17 output pin_1
	MFS6_SIN_0		Multi-function serial ch.6 serial data input pin_0
	TRACE_CLK_0		Trace clock output pin_0
	PWU_AN6		Partial wakeup ADC analog 6 input pin
65	P1_05	C	GPIO port
	ADC0_AN16		ADC ch.16 analog input pin
	EINT14_0		External interrupt ch.14 input pin_0
	SG3_SGO_0		Sound generator ch.3 SGO output pin_0
	BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_1		Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_1
	OCU9_OUT0_1		Output compare9 ch.0 output pin_1
	ICU9_IN0_1		Input capture9 ch.0 input pin_1
	RLT2_TIN_1		Reload timer ch.2 event input pin_1
	CAN3_RX_0		CAN ch.3 reception data input pin_0
	MFS7_SOT_0		Multi-function serial ch.7 serial data output pin_0
	MFS7_SDA		I2C ch.7 serial data I/O pin
	TRACE_CTL_0		Trace control output pin_0
	PWU_AN7		Partial wakeup ADC analog 7 input pin
66	P1_06	C	GPIO port

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
70	AVRL5	-	ADC low reference voltage pin
71	AVRH5	-	ADC high reference voltage pin
72	VCC5	-	+5.0 V power supply pin
73	VSS	A	GND
74	P1_08	A	GPIO port
	ADC0_TRG0_1		ADC external trigger ch.0 input pin_1
	EINT16_0		External interrupt ch.16 input pin_0
	BT5_TIOA11_0		Base timer5 ch.11 TIOA output pin_0
	OCU10_OUT0_0		Output compare10 ch.0 output pin_0
	ICU10_IN1_0		Input capture10 ch.1 input pin_0
	RLT3_TIN_0		Reload timer ch.3 event input pin_0
	MFS7_CS0_0		Multi-function serial ch.7 serial chip select 0 I/O pin_0
	IND0_OUT_1		Indicator PWM output pin_1
75	VSS	-	GND
76	VCC5	-	+5.0 V power supply pin
77	P1_09	A	GPIO port
	ADC0_TRG0_0		ADC external trigger ch.0 input pin_0
	EINT9_4		External interrupt ch.9 input pin_4
	BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_0		Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_0
	OCU10_OUT1_0		Output compare10 ch.1 output pin_0
	RLT3_TOT_0		Reload timer ch.3 output pin_0
	MFS7_CS1_0		Multi-function serial ch.7 serial chip select 1 output pin_0
	RTC0_WOT		RTC overflow output pin
	SYSC0_CLK_0		System clock output pin_0
78	DVSS	-	SMC high current port GND pin
79	DVCC	-	SMC high current port power supply pin
80	P1_10	O	GPIO port
	ADC0_AN24		ADC ch.24 analog input pin
	SMC0_PWM1P		Stepper Motor Controller ch.0 PWM1P output pin
	EINT17_0		External interrupt ch.17 input pin_0
	BT6_TIOA12_0		Base timer6 ch.12 TIOA output pin_0
81	P1_11	O	GPIO port
	ADC0_AN25		ADC ch.25 analog input pin
	SMC0_PWM1M		Stepper Motor Controller ch.0 PWM1M output pin
	EINT11_4		External interrupt ch.11 input pin_4
	BT6_TIOA13_0		Base timer6 ch.13 TIOA output pin_0
82	P1_12	O	GPIO port
	ADC0_AN26		ADC ch.26 analog input pin
	SMC0_PWM2P		Stepper Motor Controller ch.0 PWM2P output pin
	EINT18_0		External interrupt ch.18 input pin_0
	BT7_TIOA14_0		Base timer7 ch.14 TIOA output pin_0
	MFS0_SOT_0		Multi-function serial ch.0 serial data output pin_0
	MFS8_SDA		I2C ch.8 serial data I/O pin

LQFP144/ TEQFP144			
		I/O Circuit Type	Function Description
			GPIO port
			ADC ch.27 analog input pin
	_PWM2M		Stepper Motor Controller ch.0 PWM2M output pin
	INT12_4	O	External interrupt ch.12 input pin_4
	BT7_TIOA15_0		[redacted]
	MFS0_SCK_0		Multi-function serial ch.0 clock I/O pin_0
	MFS8_SCL		I2C ch.8 clock I/O pin
[redacted]			GPIO port
	ADC0_AN28		[redacted]
[redacted]		O	upt ch.19 input pin_0

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
92	P1_20	O	GPIO port
	ADC0_AN34		ADC ch.34 analog input pin
	SMC2_PWM2P		Stepper Motor Controller ch.2 PWM2P output pin
	EINT20_0		External interrupt ch.20 input pin_0
	BT11_TIOA22_0		Base timer11 ch.22 TIOA output pin_0
	MFS9_SIN_0		Multi-function serial ch.9 serial data input pin_0
93	P1_21	O	GPIO port
	ADC0_AN35		ADC ch.35 analog input pin
	SMC2_PWM2M		Stepper Motor Controller ch.2 PWM2M output pin
	EINT20_4		External interrupt ch.20 input pin_4
	BT11_TIOA23_0		Base timer11 ch.23 TIOA output pin_0
	MFS10_SOT_0		Multi-function serial ch.10 serial data output pin_0
	MFS10_SDA		I2C ch.10 serial data I/O pin
94	P1_22	O	GPIO port
	ADC0_AN36		ADC ch.36 analog input pin
	SMC3_PWM1P		Stepper Motor Controller ch.3 PWM1P output pin

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
112			

LQFP144/ TEQFP144			
Pin No.	Pin Name	I/O Circuit Type	Function Description
122			

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
129	P2_17	P	GPIO port
	MDATA3		External BUS Interface data I/O pin
	LCD0_SEG24		LCD controller segment output pin
	EINT23_5		External interrupt ch.23 input pin_5
	MFS4_SCK_0		Multi-function serial ch.4 clock I/O pin_0
	MFS4_SCL		I2C ch.4 clock I/O pin
	LCDD2		LCD BUS interface data I/O pin
130	P2_18	P	GPIO port
	MDATA4		External BUS Interface data I/O pin
	LCD0_SEG23		LCD controller segment output pin
	EINT0_0		External interrupt ch.0 input pin_0
	MFS4_SIN_0		Multi-function serial ch.4 serial data input pin_0
	LCDD3		LCD BUS interface data I/O pin
131	P2_19	P	GPIO port

LQFP144/ TEQFP144			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
139	P2_25	P	GPIO port
	MAD3		External BUS Interface address output pin
	LCD0_SEG16		LCD controller segment output pin
	EINT1_0		External interrupt ch.1 input pin_0
	MFS1_SIN_0		Multi-function serial ch.1 serial data input pin_0
	LCDD7		LCD BUS interface data I/O pin
140	P2_26	P	GPIO port
	MAD4		External BUS Interface address output pin
	LCD0_SEG15		LCD controller segment output pin
	EINT5_1		External interrupt ch.5 input pin_1
	MFS1_CS0_0		Multi-function serial ch.1 serial chip select 0 I/O pin_0
	MFS0_CS0_1		Multi-function serial ch.0 serial chip select 0 I/O pin_1
	LCDD8		LCD BUS interface data I/O pin
141	P2_27	P	GPIO port
	MAD5		External BUS Interface address output pin
	LCD0_SEG14		LCD controller segment output pin
	EINT11_1		External interrupt ch.11 input pin_1
	MFS1_CS1_0		Multi-function serial ch.1 serial chip select 1 output pin_0
	MFS0_SOT_1		Multi-function serial ch.0 serial data output pin_1

5.1.3 LQFP120/ TEQFP120

Table 5-1-3: Pin Descriptions of LQFP120/ TEQFP120 5

LQFP120/ TEQFP120			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
1	VCC53_1	-	+3.3 V/ +5.0 V selection power supply pin (1)
2	P0_06	P	GPIO port
	LCD0_SEG5		LCD controller segment output pin
	EINT8_2		External interrupt ch.8 input pin_2
	BT3_TIOA7_1		Base timer3 ch.7 TIOA output pin_1
	CS#		LCD BUS interface chip select output pin
3	VCC53_1	-	+3.3 V/ +5.0 V selection power supply pin (1)
4	VSS	-	GND
5	P0_07	P	GPIO port
	LCD0_SEG4		LCD controller segment output pin
	EINT18_2		External interrupt ch.18 input pin_2
	MFS4_SOT_1		Multi-function serial ch.4 serial data output pin_1
	WR#		LCD BUS interface write enable output pin
6	P0_08	P	GPIO port
	LCD0_SEG3		LCD controller segment output pin
	EINT19_2		External interrupt ch.19 input pin_2
	MFS4_SCK_1		Multi-function serial ch.4 clock I/O pin_1
	RD#		LCD BUS interface read enable output pin
7	P0_09	P	GPIO port
	LCD0_SEG2		LCD controller segment output pin
	EINT20_2		External interrupt ch.20 input pin_2
	MFS4_SIN_1		Multi-function serial ch.4 serial data input pin_1
8	P0_10	P	GPIO port
	LCD0_SEG1		LCD controller segment output pin
	EINT21_2		External interrupt ch.21 input pin_2
	MFS4_CS0_1		Multi-function serial ch.4 serial chip select 0 I/O pin_1
	RS		LCD BUS interface register select output pin
9	P0_11	P	GPIO port
	LCD0_SEG0		LCD controller segment output pin
	EINT22_2		External interrupt ch.22 input pin_2
	MFS4_CS1_1		Multi-function serial ch.4 serial chip select 1 output pin_1
	RES#		LCD BUS interface reset control output pin
10	P0_12	A	GPIO port
	EINT23_2		

LQFP120/ TEQFP120			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
15	P0_15 DDRHSSPI1_SDATA1	M	GPIO port

LQFP120/ TEQFP120			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
54	P1_01	A	GPIO port
	ADC0_AN12		ADC ch.12 analog input pin
	EINT11_0		External interrupt ch.11 input pin_0
	SG1_SGO_0		Sound generator ch.1 SGO output pin_0
	BT2_TIOA5_0		Base timer2 ch.5 TIOA output pin_0
	OCU1_OUT1_0		Output compare1 ch.1 output pin_0
	ICU2_IN1_0		Input capture2 ch.1 input pin_0
	QPRC9_ZIN		Quadrature Position and Revolution Counter ch.9 ZIN input pin
	RLT16_TOT_0		Reload timer ch.16 output pin_0
	CAN2_TX_0		CAN ch.2 transmission data output pin_0
	PWU_AN3		Partial wakeup ADC analog 3 input pin
55	P1_02	C	GPIO port
	ADC0_AN13		ADC ch.13 analog input pin
	EINT12_0		External interrupt ch.12 input pin_0
	BT3_TIOA6_0		Base timer3 ch.6 TIOA output pin_0
	OCU2_OUT0_0		Output compare2 ch.0 output pin_0
	ICU8_IN0_0		Input capture8 ch.0 input pin_0
	PWU_AN4		Partial wakeup ADC analog 4 input pin
56	AVCC5	-	Analog power supply pin
57	AVSS	-	Analog GND pin
58	AVRL5	-	ADC low-reference voltage pin
59	AVRH5	-	ADC high-reference voltage pin
60	VCC5	-	+5.0 V power supply pin
61	VSS	A	GND
62	VSS	-	GND
63	VCC5	-	+5.0 V power supply pin
64	P1_09	A	GPIO port
	ADC0_TRG0_0		ADC external trigger ch.0 input pin_0
	EINT9_4		External interrupt ch.9 input pin_4
	BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_0		Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_0
	OCU10_OUT1_0		Output compare10 ch.1 output pin_0
	RTC0_WOT		RTC overflow output pin
	SYSC0_CLK_0		System clock output pin_0
65	DVSS	-	SMC high current port GND pin
66	DVCC	-	SMC high current port power supply pin
67	P1_10	O	GPIO port
	ADC0_AN24		ADC ch.24 analog input pin
	SMC0_PWM1P		Stepper Motor Controller ch.0 PWM1P output pin
	EINT17_0		External interrupt ch.17 input pin_0
	BT6_TIOA12_0		Base timer6 ch.12 TIOA output pin_0
68	P1_11	O	GPIO port
	ADC0_AN25		ADC ch.25 analog input pin
	SMC0_PWM1M		Stepper Motor Controller ch.0 PWM1M output pin
	EINT11_4		External interrupt ch.11 input pin_4
	BT6_TIOA13_0		Base timer6 ch.13 TIOA output pin_0

LQFP120/ TEQFP120			
Pin No.	Pin Name	I/O Circuit Type	Function Description

LQFP120/ TEQFP120			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
87	P1_26	O	GPIO port
	ADC0_AN40		ADC ch.40 analog input pin
	EINT2_5		External interrupt ch.2 input pin_5
	BT13_TIOA27_0		Base timer13 ch.27 TIOA output pin_0
88	P1_27	O	GPIO port
	ADC0_AN41		ADC ch.41 analog input pin
	EINT3_5		External interrupt ch.3 input pin_5
	BT14_TIOA28_0		Base timer14 ch.28 TIOA output pin_0
89	P1_31	O	GPIO port
	ADC0_AN45		ADC ch.45 analog input pin
	EINT7_5		External interrupt ch.7 input pin_5
	BT12_TIOB24/BT13_TIOB26/BT14 _TIOB28/BT15_TIOB30_0		Base timer12/13/14/15 ch.24/26/28/30 TIOB input pin_0
90	DVSS	-	SMC high current port GND pin
91	DVCC	-	SMC high current port power supply pin
92	VSS	-	GND
93	VCC53_1	-	+3.3 V/ +5.0 V selection power supply pin (1)
94	P2_02	Q	General-purpose input port
	LCD0_V3		LCD controller Reference Voltage V3 input pin
	EINT2_1		External interrupt ch.2 input pin_1
95	P2_03	A	GPIO port
	LCD0_V2		LCD controller Reference Voltage V2 input pin
	EINT10_5		

LQFP100/ TEQFP100			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
17	P0_17	M	GPIO port
	EINT4_3		External interrupt ch.4 input pin_3
	MFS2_CS1_0		Multi-function serial ch.2 serial chip select 1 output pin_0
	MFS9_CS1_2		Multi-function serial ch.9 serial chip select 1 output pin_2
18	VCC53_2	-	+3.3 V/ +5.0 V selection power supply pin (2)
19	VSS	-	GND
20	VSS	-	GND
21	P0_20	M	GPIO port
	EINT7_3		External interrupt ch.7 input pin_3
22	P0_23	M	GPIO port
	ADC0_AN1		ADC ch.1 analog input pin
	EINT9_3		External interrupt ch.9 input pin_3
23	VCC53_2	-	+3.3 V/ +5.0 V selection power supply pin (2)
24	VSS	-	GND
25	VCC53_2	-	+3.3 V/ +5.0 V selection power supply pin (2)
26	VSS	-	GND
27	X1	K	Main clock oscillation output pin
28	X0	K	Main clock oscillation input pin
29	MODE	G	Mode pin
30	RSTX	H	External reset input pin
31	JTAG_NTRST	D	JTAG test reset input pin
32	JTAG_TDO	F	JTAG test data output pin
33	JTAG_TDI	E	JTAG test data input pin
34	JTAG_TCK		

LQFP100/ TEQFP100			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
59	P1_12	O	GPIO port
	ADC0_AN26		ADC ch.26 analog input pin
	SMC0_PWM2P		Stepper Motor Controller ch.0 PWM2P output pin
	EINT18_0		External interrupt ch.18 input pin_0
	BT7_TIOA14_0		Base timer7 ch.14 TIOA output pin_0
	MFS0_SOT_0		Multi-function serial ch.0 serial data output pin_0
	MFS8_SDA		I2C ch.8 serial data I/O pin
60	P1_13	O	GPIO port
	ADC0_AN27		ADC ch.27 analog input pin
	SMC0_PWM2M		Stepper Motor Controller ch.0 PWM2M output pin
	EINT12_4		E3 11.4 reW* nq275.57 518.83 263.93 11.4 reW* nBT/F2 9 Tf1 0

F 1180.7n BT /F2 3(r 9 Tf 8 1400 1 O916.7n BT /F20.94 [(E3 11.4 re W*n 6 9.7188.06 /F229INT 1155.43010)5

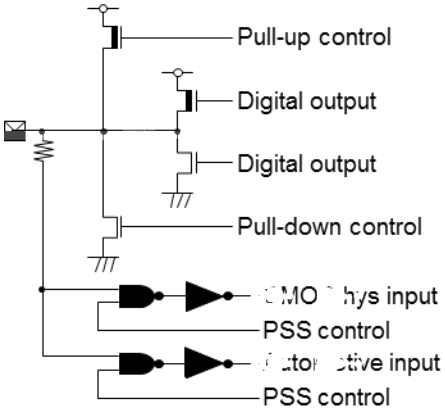
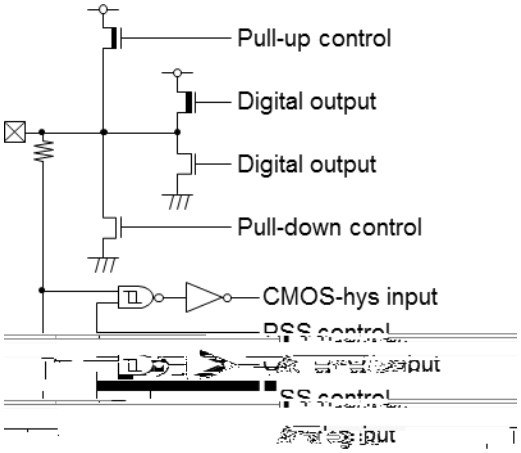
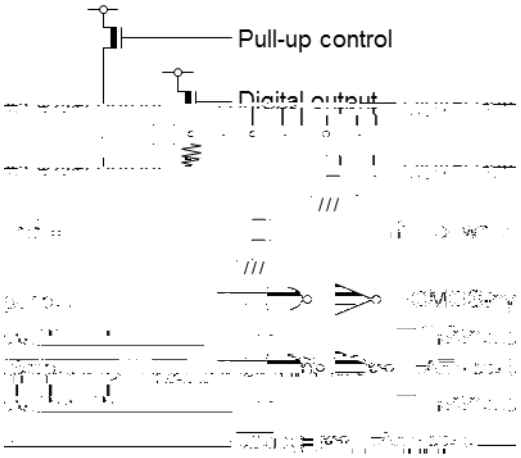
LQFP100/ TEQFP100			
Pin No.	Pin Name	I/O Circuit Type	Function Description

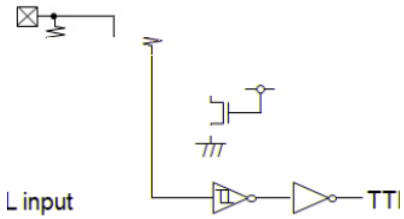
gpg[t (gp)9(inc)-5(0 g[ )]TJETQq542Q9q5 649.71 0 2 7.63 82.8 r8 0.48 30 ref*234.390.19q54e174 660.58 Tm0 g[ )]TJE ref55 00.78 155.78 9.78.48 0.48Tre

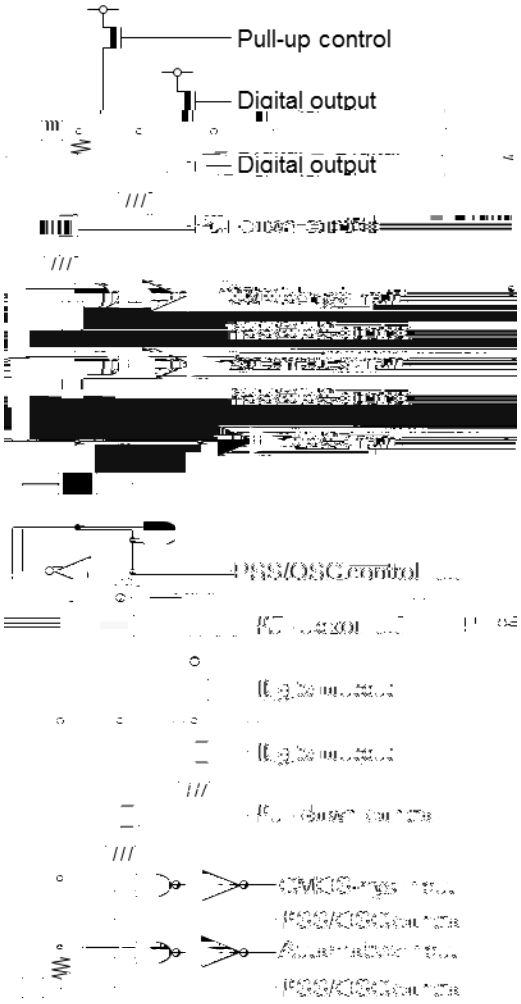
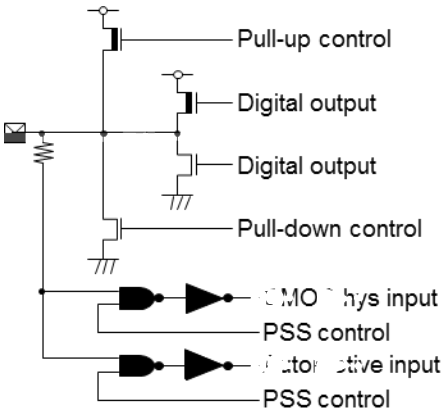
LQFP100/ TEQFP100			
Pin No.	**Pin Name**	**I/O Circuit Type**	**Function Description**
82	P2_05	A	GPIO port
	I2S0_SD_1		I2S ch.0 serial data I/O pin_1
	LCD0_V0		LCD controller Reference Voltage V0 input pin
	EINT12_5		External interrupt ch.12 input pin_5
	BT12_TIOA25_1		Base timer12 ch.25 TIOA output pin_1
	MFS2_SCK_1		Multi-function serial ch.2 clock I/O pin_1
83	P2_06	P	GPIO port

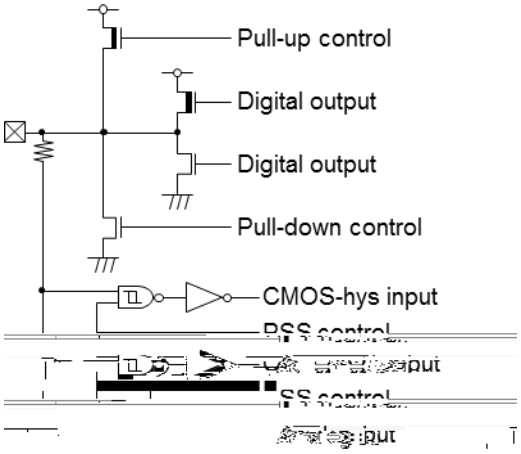
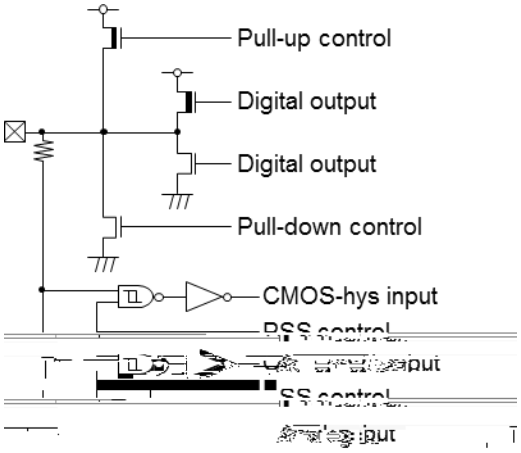
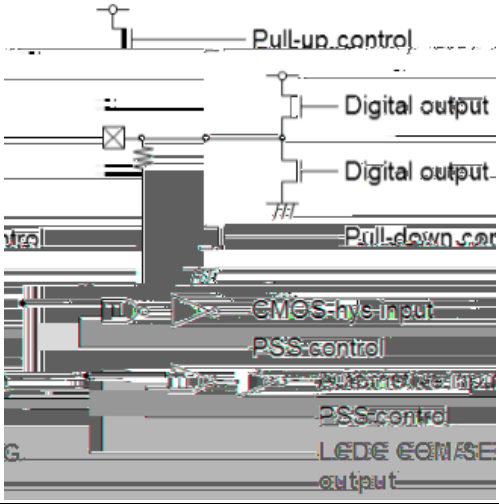
5.2 I/O Circuit Type

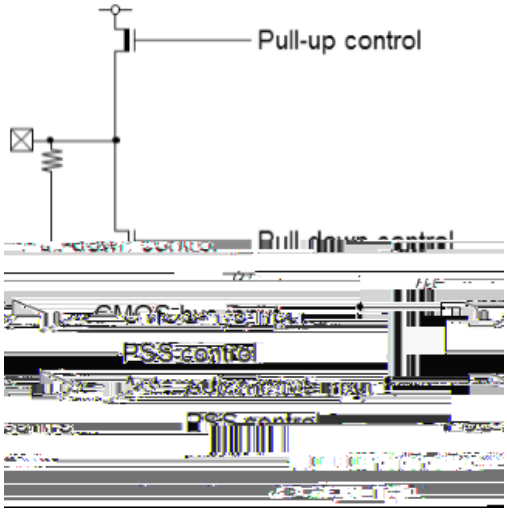
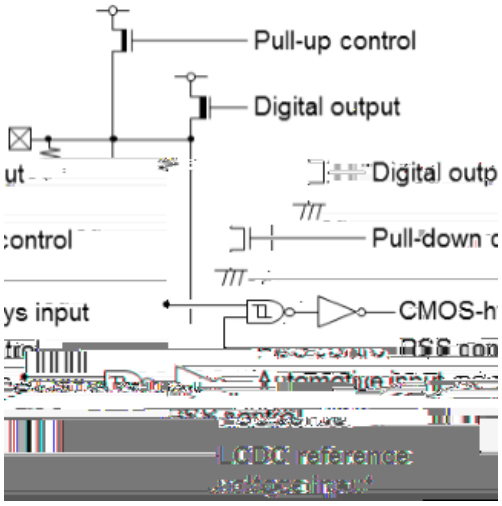
Table 5-2: I/O Circuit Types

Type	Circuit	Remark
A		GPIO port Output 1 mA, 2 mA, or 5 mA selectable -up resistor control with pull-down resistor control CMOS hysteresis or Automotive hysteresis input selectable
B		GPIO port with analog input Output 1 mA, 2 mA, or 5 mA selectable -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable
C		GPIO port with analog input Output 1 mA, 2 mA, 3 mA(I2C), or 5 mA selectable -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable

Type	Circuit	Remark
D		JTAG_NTRST -down resistor TTL hysteresis input
E		JTAG_TDI/TCK/TMS -

Type	Circuit	Remark
L		Sub oscillation I/O shared GPIO port Output 1 mA, 2 mA, or 5 mA selectable -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable
M		GPIO port Output 1 mA or 2 mA selectable (VCC53_2 = 4.5 V to 5.5 V) Output 5 mA or 15 mA selectable (VCC53_2 = 3.0 V to 3.6 V) -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable

Type	Circuit	Remark
N		GPIO port with analog input Output 1 mA or 2 mA selectable (VCC53_2 = 4.5 V to 5.5 V) Output 5 mA or 15 mA selectable (VCC53_2 = 3.0 V to 3.6 V) -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable
O		GPIO port with analog input Output 1 mA, 2 mA, 5 mA, or 30 mA selectable 50 -up resistor control -down resistor control CMOS hysteresis or Automotive hysteresis input selectable
P		GPIO port with LCDC COM/SEG output Output 1 mA, 2 mA or 5 mA selectable 50 -up resistor control 50 -down resistor control CMOS hysteresis or Automotive hysteresis input selectable

Type	Circuit	Remark
Q		General-purpose input port with LCDC reference voltage input 50 -up resistor control 50 -down resistor control CMOS hysteresis or Automotive hysteresis input selectable
R		GPIO port with LCDC reference voltage input Output 1 mA, 2 mA, or 5 mA selectable 50 -up resistor control 50 -down resistor control CMOS hysteresis or Automotive hysteresis input selectable

5.3 Input Level Setting/ Output Drive Capacity Setting

(1) When power supply pin of each I/O is used at 5V

Table 5-3-1: Input Level Setting/ Output Drive Capacity Setting

Pin No. of LQFP/TEQFP Package			Port Name	Input Level Setting	Output Drive Capacity Setting	Power of Pin (pin group)	Remark
100-pin	120-pin	144					

Pin No. of LQFP/TEQFP Package	Port Name	Input Level Setting	Output Drive Capacity Setting	Power of Pin (pin group)	

(2) When power supply pin of each I/O is used at 3.3V

Table 5-3-2: Input Level Setting/ Output Drive Capacity Setting

Pin No. of LQFP/TEQFP Package				Port name	Input Level Setting		Output Drive Capacity Setting				Power of Pin (pin group)	Remark
100-pin	120-pin	144-pin	176-pin									
-	-	2	2	P0_00	CMOS-hys	Automotive	0.5 mA	1 mA	-	2 mA		
-	-	3	3	P0_01	CMOS-hys	Automotive	0.5					

V_{CC53_1}

Pin No. of LQFP/TEQFP Package				Port name	Input Level Setting	Output Drive Capacity Setting	Power of Pin (pin group)	Remark
100-pin	120-pin	144-pin	176-pin					
-	-	67	81	P1_07				

Pin No. of LQFP/TEQFP Package	Port name

6. Block Diagram

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC5}	V_{SS}-0.3	V_{SS}+6.0	V	
	V_{CC53_1}	V_{SS}-0.3	V_{SS}+6.0	V	V_{CC53_1}

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
H-level maximum output current*3	I_{OH1}	-	-3.5	mA	When setting is 1 mA ALL GPIO*6
	I_{OH2}	-	-7	mA	When setting is 2 mA ALL GPIO*6
	I_{OH3}	-	-10	mA	When setting is 5 mA GPIO of V_{CC5}/V_{CC53_1}/DV_{CC}*6
	I_{OH3}	-	-10	mA	When setting is 5 mA GPIO of V_{CC53_2}*6
	I_{OH4}	-	-20	mA	When setting is 15 mA GPIO of V_{CC53_2}*6
	I_{OH5}	-	-40	mA	When setting is 30 mA GPIO of DV_{CC}*6
H-level average output current*4	I_{OHAV1}	-	-1	mA	When setting is 1 mA ALL GPIO*6
	I_{OHAV2}	-	-2	mA	When setting is 2 mA ALL GPIO*6
	I_{OHAV3}	-	-5	mA	When setting is 5 mA GPIO of V_{CC5}/V_{CC53_1}/DV_{CC}*6
	I_{OHAV3}	-	-5	mA	When setting is 5 mA GPIO of V_{CC53_2}*6
	I_{OHAV4}	-	-15	mA	When setting is 15 mA GPIO of V_{CC53_2}*6
	I_{OHAV5}	-	-30	mA	When setting is 30 mA GPIO of DV_{CC}*6
H-level total output current*5	$_{OH1}$				

*5

*A: Relevant pins: All general-purpose ports and analog input pins
Corresponding pins: all general-purpo(e)9(n)-3(e(rBT0 0 1(:)Is)4(a)-5(n(:)BT1 0 0 1 307.51 684.2 5097[( )] TJETBT1 0 0 1 68. 0 0 1 61.

7.2 Recommended Operating Conditions

(1) Recommended Operation Conditions for S6J33nnnXnnnnnnnn (X=S, T, U, V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC5}	4.5	5.5	V	Recommended operation assurance range (case1) *1
	V_{CC53_1}	4.5	5.5	V	
		3.0	3.6	V	
	V_{CC53_2}	4.5	5.5	V	
		3.0	3.6	V	
	DV_{CC}	4.5	5.5	V	
	AV_{CC5}	4.5	5.5	V	
	V_{CC5}	3.0	3.6	V	Recommended operation assurance range (case2) *1
	V_{CC53_1}	3.0	3.6	V	
	V_{CC53_2}	3.0	3.6	V	
	DV_{CC}	3.0	3.6	V	
	AV_{CC5}	3.0	3.6	V	
	V_{CC5}	2.7	5.5	V	Operation assurance range*2
	V_{CC53_1}	2.7	5.5	V	
	V_{CC53_2}	2.7	5.5	V	
	DV_{CC}	2.7	5.5	V	
	AV_{CC5}	2.7	5.5	V	
Smoothing capacitor*3	C_S	4.7		uF	Tolerance of up to ±40%
Operating temperature	T_A	-40	105	°C	

(2) Recommended Operation Conditions for S6J33nnnXnnnnnnnn (X=A, E, C, G)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC5}	4.5	5.5	V	Recommended operation assurance range (case1) *1
	V_{CC53_1}	4.5	5.5	V	
		3.0	3.6	V	
	V_{CC53_2}	4.5	5.5	V	
		3.0	3.6	V	
	DV_{CC}	4.5	5.5	V	
	AV_{CC5}	4.5	5.5	V	
	V_{CC5}	3.0	3.6	V	Recommended operation assurance range (case2) *1
	V_{CC53_1}	3.0	3.6	V	
	V_{CC53_2}	3.0	3.6	V	
	DV_{CC}	3.0	3.6	V	
	AV_{CC5}	3.0	3.6	V	
	V_{CC5}	3.0	3.6	V	Recommended operation assurance range (case3) *1
	V_{CC53_1}	3.0	3.6	V	
	V_{CC53_2}	3.0	3.6	V	
	DV_{CC}	4.5	5.5	V	
	AV_{CC5}	3.0	3.6	V	
	V_{CC5}	2.7	5.5	V	Operation assurance range*2
	V_{CC53_1}	2.7	5.5	V	
	V_{CC53_2}	2.7	5.5	V	
	DV_{CC}	2.7	5.5	V	
	AV_{CC5}	2.7	5.5	V	
Smoothing capacitor*3	C_S	4.7		uF	Tolerance of up to ±40%
Operating temperature	T_A	-40	105	°C	

Notes:

**1: Recommendation of S6J3360/S6J3370 Series power supply voltage combination is as follows.*

	VCC5 [V]	VCC53_1 [V]	VCC53_2 [V]	DVCC [V]	AVCC5 [V]
Case1	5.0	5.0	5.0	5.0	5.0
	5.0	5.0	3.3	5.0	5.0
	5.0	3.3	5.0	5.0	5.0
	5.0	3.3	3.3	5.0	5.0
Case2	3.3	3.3	3.3	3.3	3.3
Case3	3.3	3.3	3.3	5.0	3.3

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name[*1]

Parameter	Symbol	Pin Name*1	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL16}	GPIO of V_{CC5} (GPIO shared I^2C)	V_{CC5}=4.5 V, I_{OL}=3.0 mA V_{CC5}=3.0 V, I_{OL}	[redacted]	-	0.4	V	

Parameter	Symbol	Pin Name*1	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
SEG0 to SEG31 output impedance	R_{VSEG}	SEGn (n=0 to 31)	-	-	-	17		
LCD leak current	I_{LCDC}	V0 to V3, COMm (m=0 to 3) SEGn (n=0 to 31)	T_A=+25℃	-0.5	-	0.5	µA	

*1: For the details of GPIO group, refer to section 5.3

7.3.2 Power Supply Current

(Condition: See Section 7.2 Recommended Operating Conditions)

7.4 AC Characteristics

7.4.1 Source Clock Timing

(Condition: See Section 7.2 Recommended Operating Conditions)

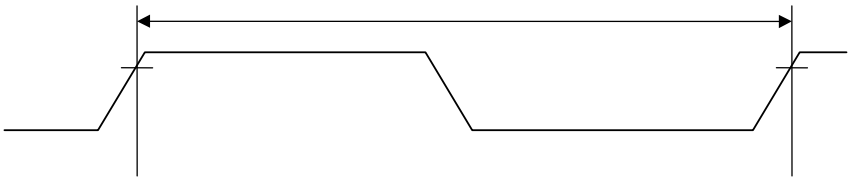
Parameter	Symbol	Pin Name	Conditions	Value	Unit

7.4.2 Sub Clock Timing

(Condition: See 7.2. Recommended Operationg Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	-	-	30.52	-	µs	

X0A and X1A clock timing



7.4.3 Internal Clock Timing

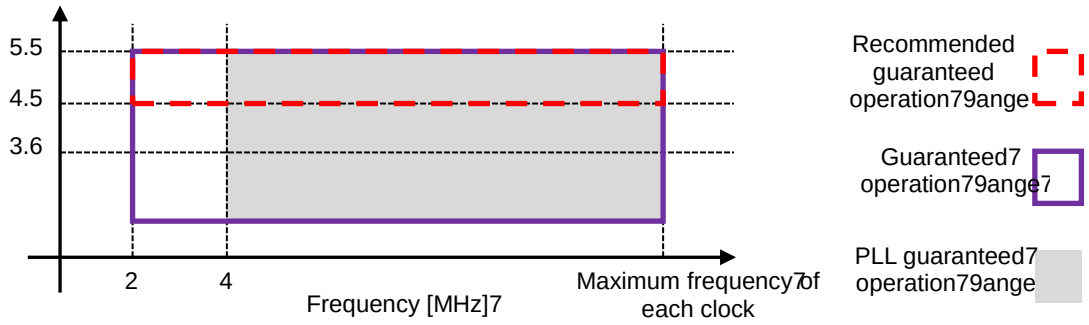
This section shows the target characteristics for internal clock timing at the current stage.

Corresponding functions for these clocks are described in Chapter 5: Clock Configuration of the S6J3360/S6J3370 series hardware manual.

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value				Unit	Remarks
				Min	Typ	Max*1	Max*2		
Internal clock frequency	$F_{SSCG0out}$	-	-	200	-	320	320	MHz	
	$F_{PLL0out}$	-	-	200	-	320	320	MHz	
	$F_{Expand_PLL0out}$	-	-	200					

Operation assurance range; Relationship between the internal clock frequency and supply voltage



Note: CPU will be79.5Noset, when7the p5Noower supply5No voltage is5No .5Noqual to or less5-6(t)9(h)-3(a)-3(n)-3(7L)7

Relationship between the oscillation clock freuency and internal clock frequency

		Internal operation clock frequency						
		Main7 clock	PLL clock					
			Multiplied7 by 1	Multiplied7 by 2	Multiplied7 by 3	Multiplied7 by 4		Multiplied7 by 20	Multiplied7 by 33
Ocillati5Noc clock freuency [MHz]	4	2	4	8	12	16		80	132

7

Oscillation circuit example

7

Note:77
For the configurati5Noon7of an os5Noc5Noillation circuit,79.5Noquest the o5Noscillator manufa5Noc5-6(tu)-5

7.4.5 Power-on Conditions

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	V_{CC5}	-	2.2	2.4	2.6	V	
Level detection hysteresis width	-	V_{CC5}	-	-	100	-	mV	
Level detection time	-	-	-	-	-	40		*1
Power off time	t_{OFF}	V_{CC5}	-	100	-	-		*2
Power ramp rate	dV/dt	V_{CC5}	V_{CC5}: 1.5 V to 2.6 V	-	-	1		*3
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	V_{CC5}	V_{CC5}: Between 2.7 V and 4.5 V	-	-	50		*4

*1: This specification is at 1 of power ramp rate.

*2: V_{CC5} must be held below 1.5 V for a minimum period of t_{OFF}.

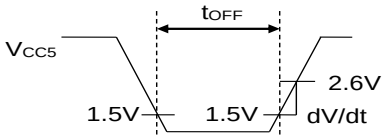
*3: Power ramp rate must be 1 V/ s or less from 1.5 V to 2.6 V.
Power-on can detect by satisfying power ramp rate and power off time.

*4: The power ramp rate specification indicates power supply fluctuation after power-on detection. When V_{CC5} voltage is between 2.7 V and 4.5 V, the power supply fluctuation is below 50 mV/us, the detection of power-on is suppressed. The power-on does not detect any power fluctuation between 4.5 V and 5.5 V.

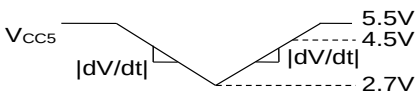
Notes:

When using the S6J3360/S6J3370 Series,*2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and any brownout event.

Power off time, Power ramp rate



Maximum ramp rate guaranteed to not generate power-on reset



7.4.6 Multi-Function Serial

7.4.6.1 UART (asynchronous serial interface) Timing (SMR:MD2-0=0b000, 0b001)

External clock selected (BGR:EXT=1)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	MFSm_SCK_x*2 (m=0 to 11)	(C_L = 20 pF, I_{OH}=-2 mA, I_{OL}=2 mA)	t_{CLK_LCPnA}*1 +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}	MFSm_SCK_x*2 (m=0 to 11)		t_{CLK_LCPnA}*1 +10	-	ns	
SCK falling time	t_F	MFSm_SCK_x*2 (m=0 to 11)		-	5	ns	
SCK rising time	t_R	MFSm_SCK_x*2 (m=0 to 11)		-	5	ns	

7.4.6.2 CSIO Timing (SMR:MD2-0=0b010)

(1) Normal synchronous transfer (SCR:SPI=0) and mark level "H" of serial clock output (SMR:SCINV=0)

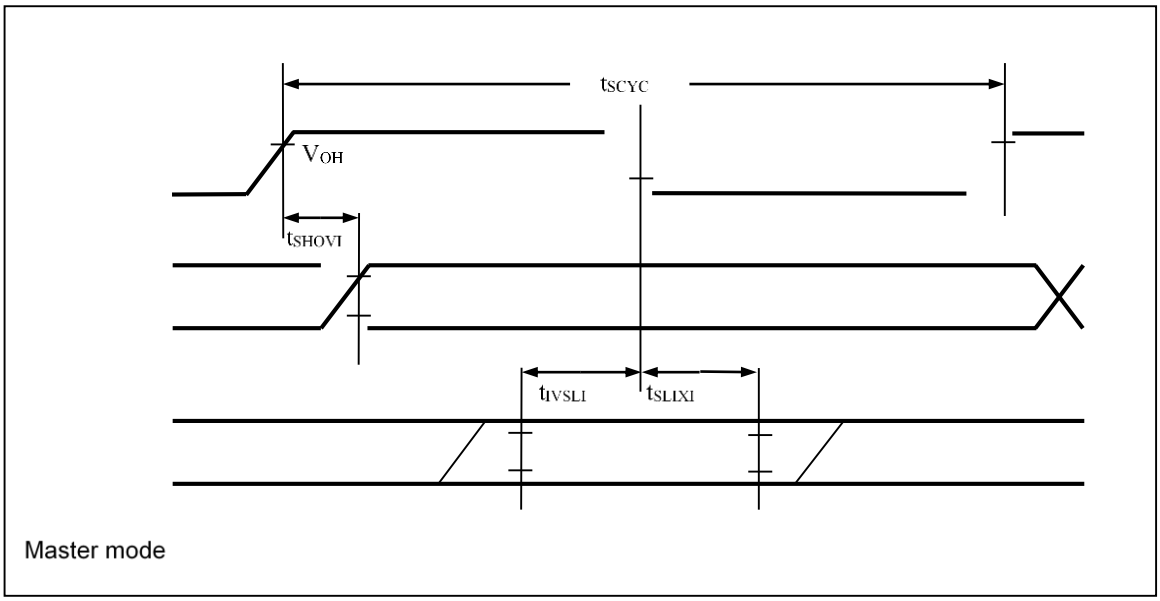
(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter Smboi

(2) Normal synchronous transfer (SCR:SPI=0) and mark level "L" of serial clock output (SMR:SCINV=1)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value	Unit



Master mode

(3) SPI supported (SCR:SPI=1), and mark level "H" of serial clock output (SMR:SCINV=0)

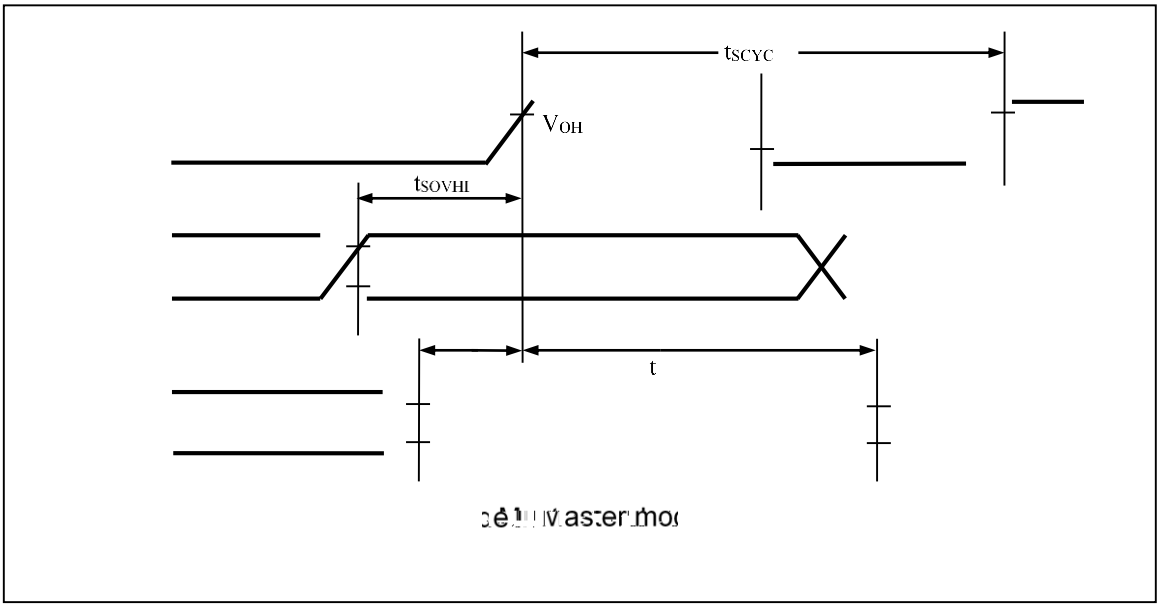
(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	MFSm_SCK_x*2 (m=0 to 11)	Master Mode (C_L = 20 pF, I_{OH}= -2 mA, I_{OL}= 2 mA)	$4t_{CLK_LCPnA}$*1	-	ns	
delay time	t_{SHOVI}	MFSm_SCK_x*2 MFSm_SOT_x*2 (m=0 to 11)		-30	30	ns	
setup time	t_{IVSLI}	MFSm_SCK_x*2 MFSm_SIN_x*2 (m=0 to 11)		31	-	ns	
SIN hold time	t_{SLIXI}	MFSm_SCK_x*2 MFSm_SIN_x*2 (m=0 to 11)		0	-	ns	
delay time	t_{SOVLI}	MFSm_SCK_x*2 MFSm_SOT_x*2 (m=0 to 11)		$2t_{CLK_LCPnA}$*1 -30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	MFSm_SCK_x*2 (m=0 to 11)	Slave Mode (C_L=20 pF, I_{OH}= -2 mA, I_{OL}= 2 mA)	$2t_{CLK_LCPnA}$*1	-	ns	
Serial clock "L" pulse width	t_{SLSH}	MFSm_SCK_x*2 (m=0 to 11)		$2t_{CLK_LCPnA}$*1	-	ns	
delay time	t_{SHOVE}	MFSm_SCK_x*2 MFSm_SOT_x*2 (m=0 to 11)		-	30	ns	
SCK setup time	t_{IVSLE}	MFSm_SCK_x*2					

(4) SPI supported (SCR:SPI=1), and mark level "L" of serial clock output (SMR:SCINV=1)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	MFSm_SCK_x[*2] (m=0 to 11)	Master Mode (C_L = 20 pF, I_{OH}= -2 mA, I_{OL}= 2 mA)	$4t_{CLK_LCPnA}$[*1]	-	ns	
-> SOT delay time	t_{SLOVI}	MFSm_SCK_x[*2] MFSm_SOT_x[*2] (m=0 to 11)		-30	30	ns	
Valid SIN -> time	t_{IVSHI}	MFSm_SCK_x[*2] MFSm_SIN_x[*2] (m=0 to 11)		31	-	ns	
-> Valid SIN hold time	t						

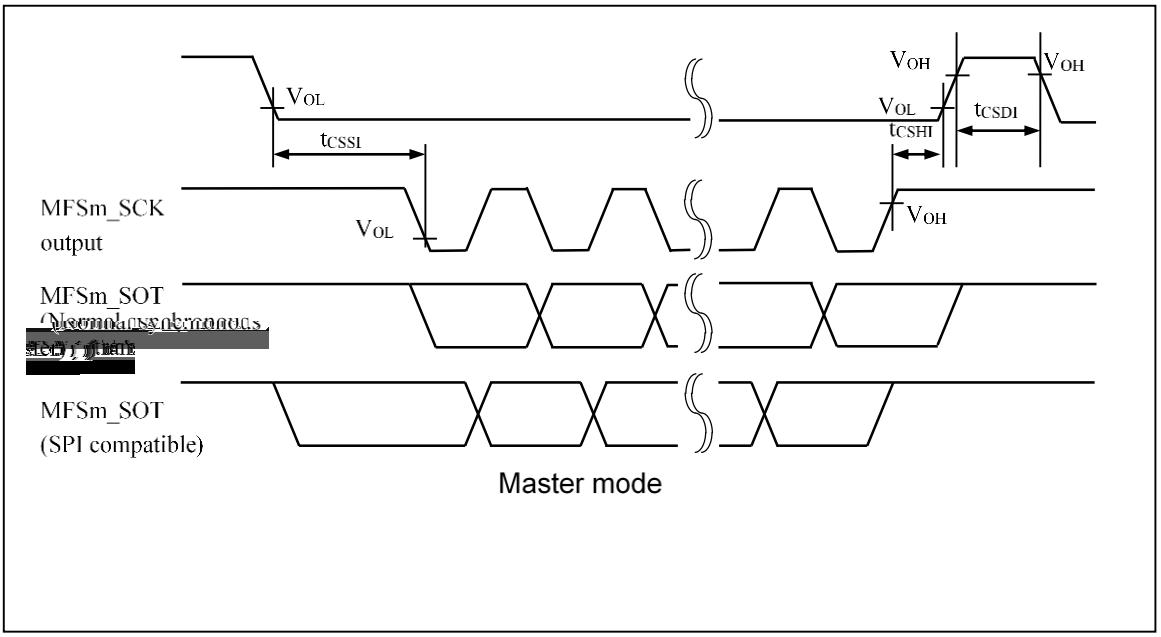

tSCYC
VOH
tSOVHI
t

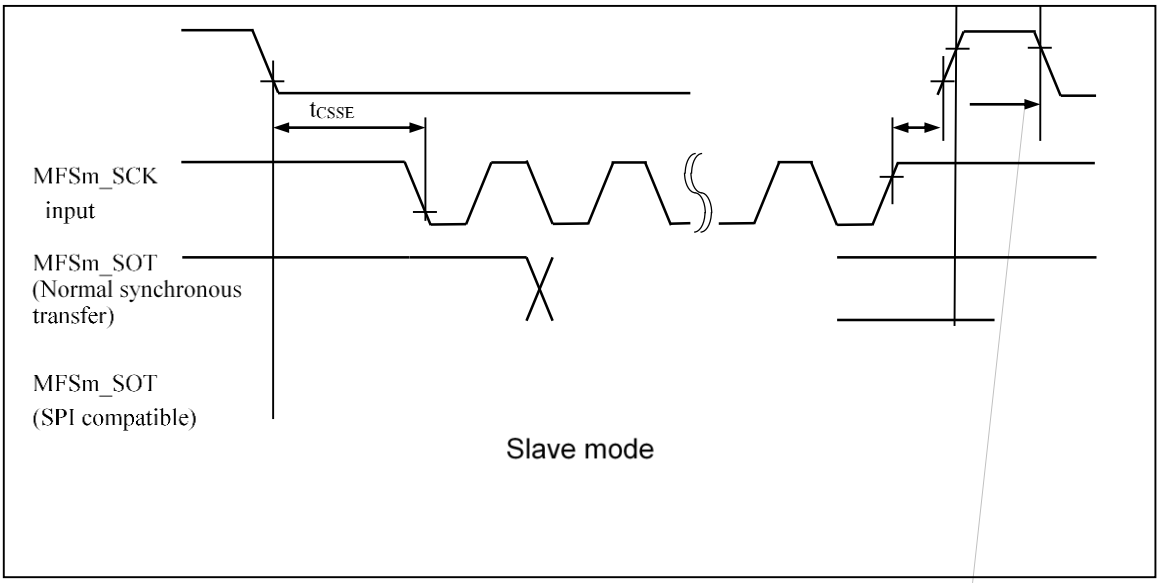
(5) Serial chip select used (SCSCR:CSEN=1)

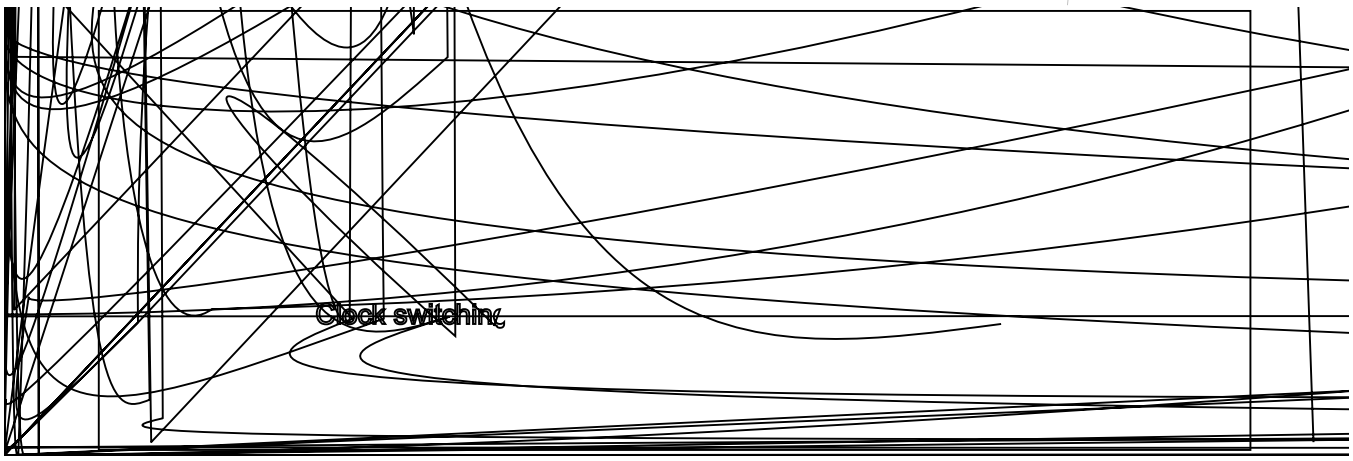
Mark level "H" of serial clock output (SMR, SCSFR:SCINV=0)

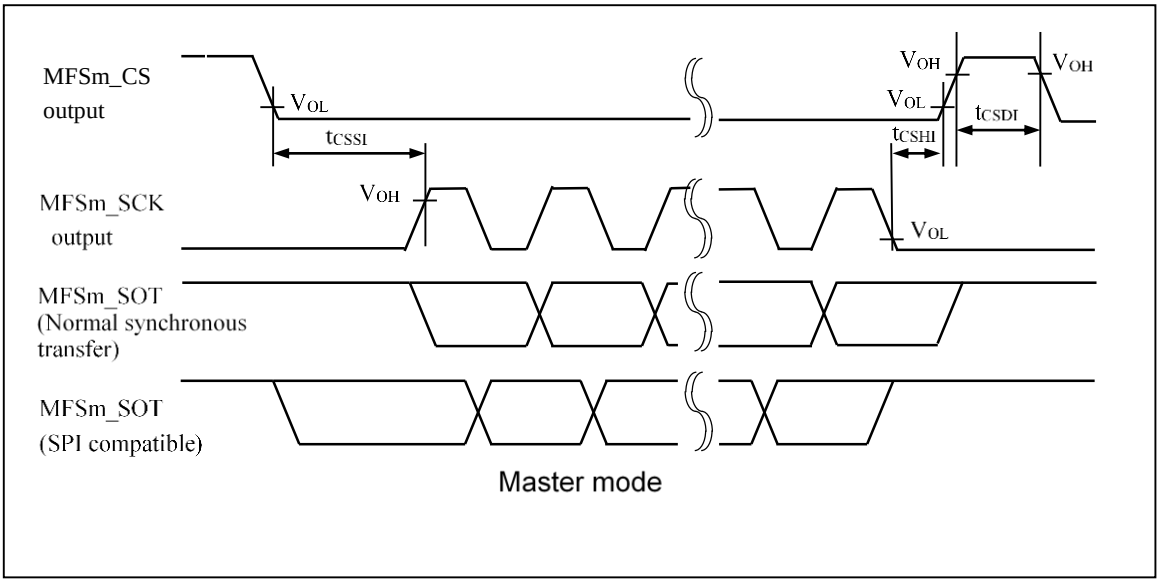
Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL=1)

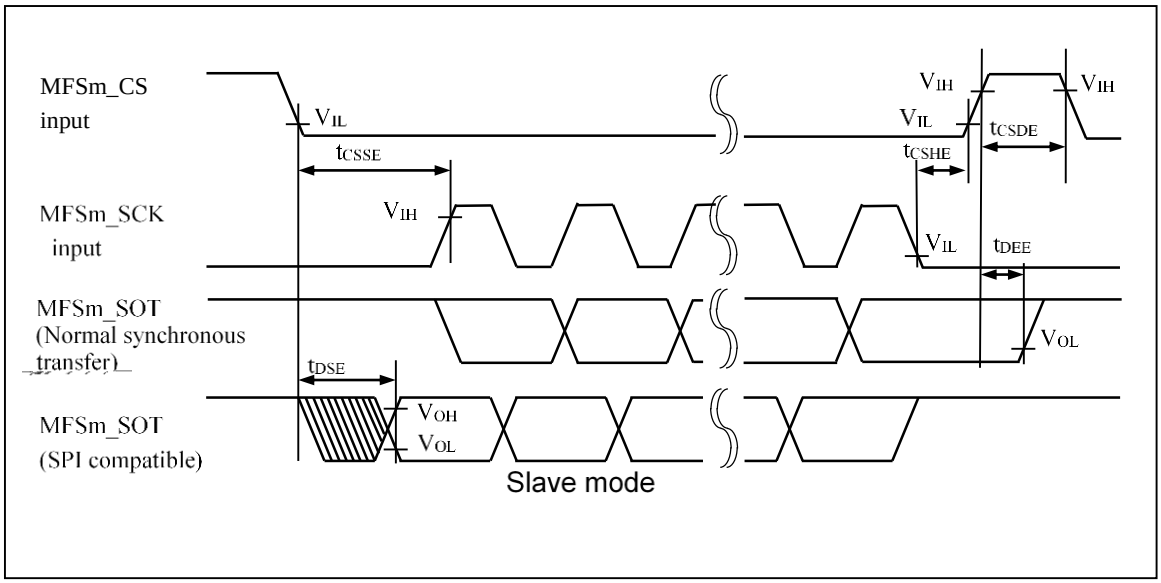
(Condition: See Section 7.2


VOH
VOH
VOL
VOL
tCSDI
tCSHI
tCSSI
MFSm_SCK
output
VOL
VOH
MFSm_SOT
MFSm_SOT
(SPI compatible)
Master mode


tCSSE
MFSm_SCK
input
MFSm_SOT
(Normal synchronous
transfer)
MFSm_SOT
(SPI compatible)
Slave mode

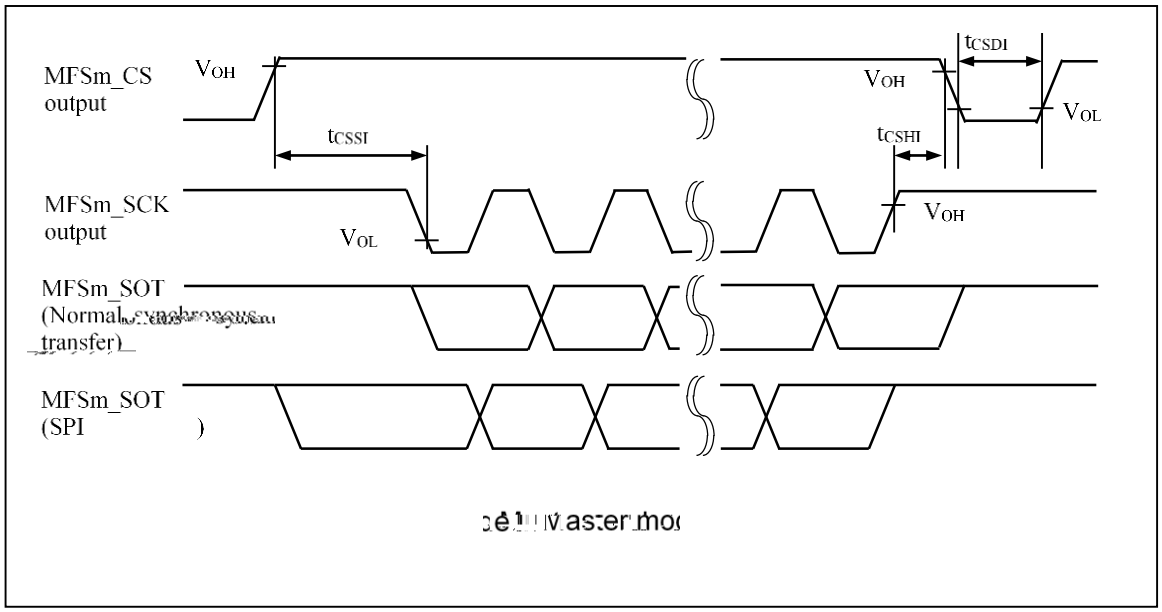

Clock switching

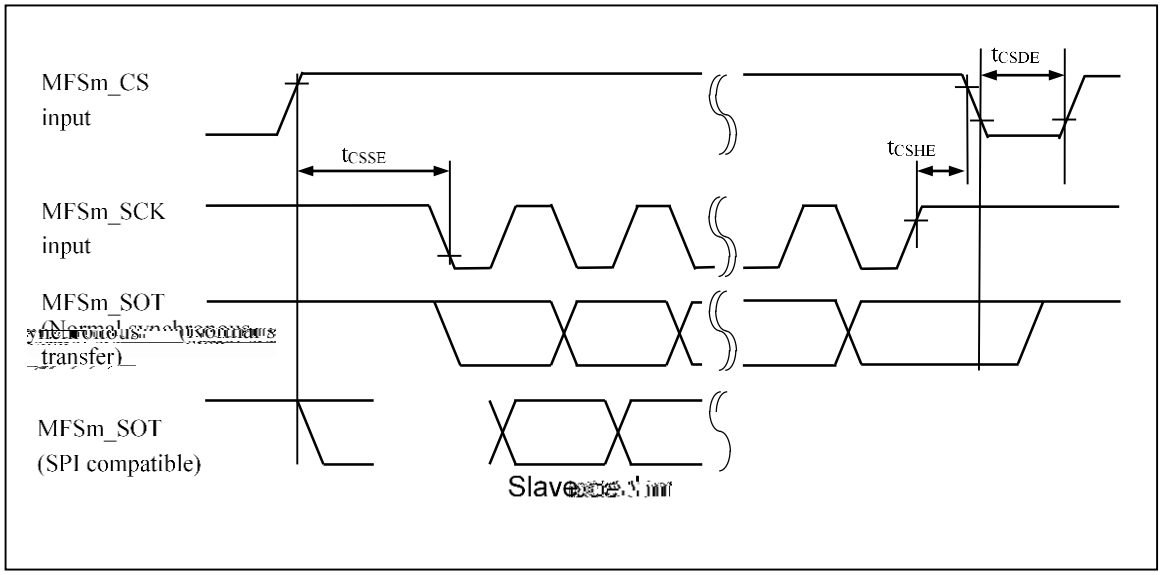

MFSm_CS
output
MFSm_SCK
output
MFSm_SOT
(Normal synchronous
transfer)
MFSm_SOT
(SPI compatible)
VOL
VOH
tCSSI
tCSDI
tCSHI
Master mode


MFSm_CS
input
MFSm_SCK
input
MFSm_SOT
(Normal synchronous
transfer)
MFSm_SOT
(SPI compatible)
VIL
VIH
VOL
VOH
tCSSE
tCSDE
tCSHE
tDEE
tDSE
Slave mode

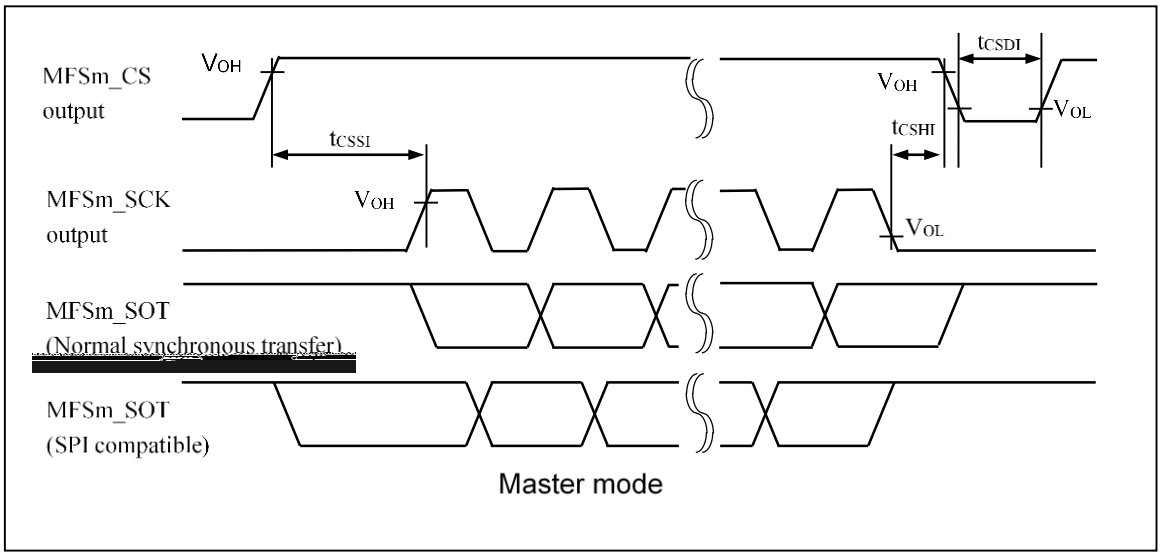
(7) Serial chip select used (SCSCR:CSEN=1)

Serial clock output signal detect level "H" (SMR, SCSFR:SCINV=0)

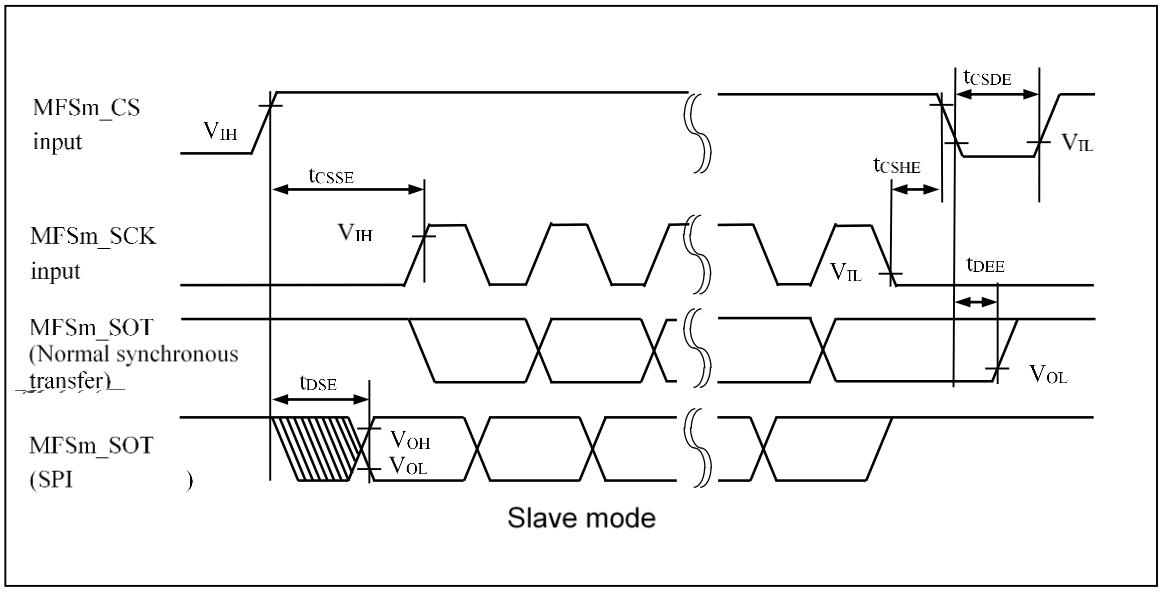

MFSm_CS
output
VOH
tCSSI
VOH
tCSDI
VOL
tCSHI
MFSm_SCK
output
VOL
VOH
MFSm_SOT
(Normal
transfer)
MFSm_SOT
(SPI
)


MFSm_CS
input
tCSSE
tCSDE
tCSHE
MFSm_SCK
input
MFSm_SOT
transfer)
MFSm_SOT
(SPI compatible)

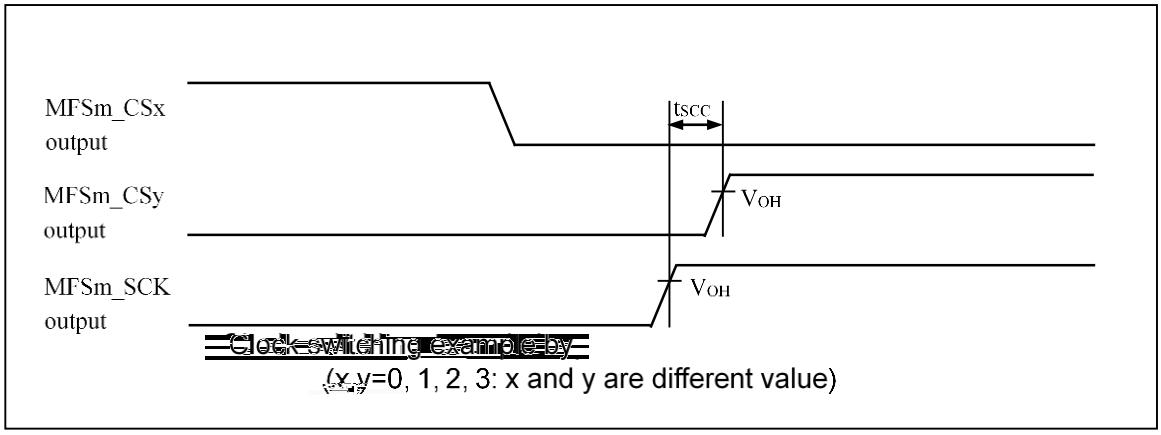
(8) Serial chip select used (SCSCR:CSEN=1)



Master mode



Slave mode



Clock switching example by
(x,y=0, 1, 2, 3: x and y are different value)

7.4.6.3 LIN Interface (v2.1) (LIN communication control interface (v2.1)) Timing (SMR:MD2-0=0b011)

External clock selected (BGR:EXT=1)

(Condition: See Section 7.2 Recommended Operating Conditions)

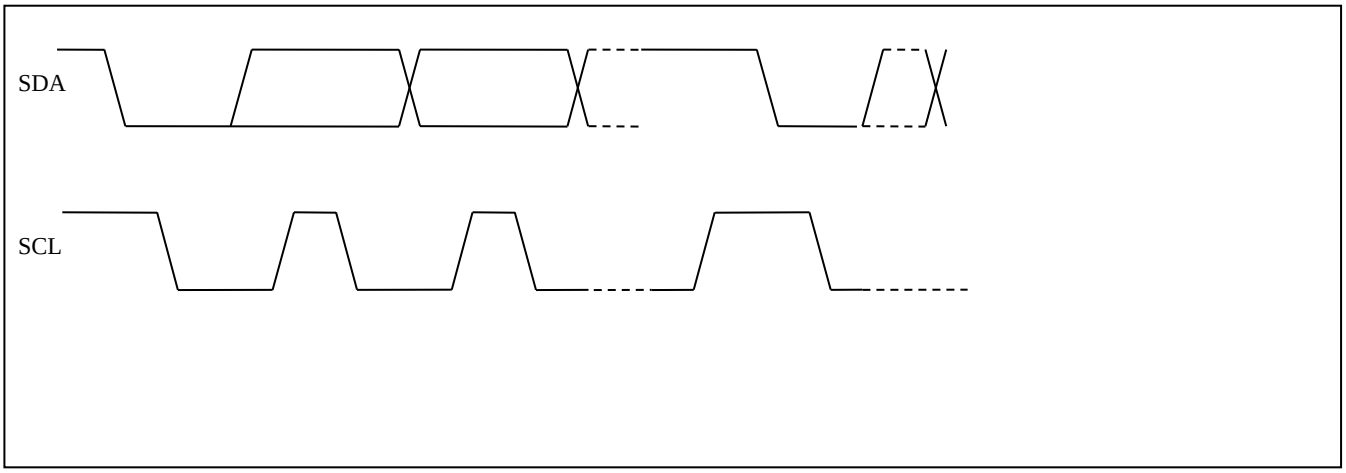
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	MFSm_SCK_x*2 (m=0 to 11)					

(C_L = 20

7.4.6.4 I^2C Timing (SMR:MD2-0=0b100)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Fast Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	MFSm_SCL (m = 0,1,4 to 11)	C_L=50pF, R=(V_p/I_{OL})*1	0	100	0	400	kHz	
Repeat "start" condition hold time	t_{HDSTA}	MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11)		4.0	-	0.6	-	µs	
Period of "L" for SCL clock	t_{LOW}	MFSm_SCL (m = 0,1,4 to 11)		4.7	-	1.3	-	µs	
Period of "H" for SCL clock	t_{HIGH}	MFSm_SCL (m = 0,1,4 to 11)		4.0	-	0.6	-	µs	
Repeat "start" condition setup time	t_{SUSTA}	MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11)		4.7	-	0.6	-	µs	
Data hold time	t_{HDDAT}	MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11)		0	3.45 *2	0	0.9 *3	µs	
Data setup time	t_{SUDAT}	MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11)		250	-	100	-	ns	
Stop condition setup time	t_{SUSTO}	MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11)		4.0	-	0.6	-	µs	


SDA
SCL

7.4.7 Timer Input

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH}, t_{TWL}	BTm_TIOBn_0, BTm_TIOBn_1					

7.4.8 QPRC Timing

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value	Unit	Remarks

7.4.9 Trigger Input

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
		EINTm_x*1 (m=0 to 23)	-	100	-	ns	
Input pulse width	t_{TRGH}, t_{TRGL}	ADC0_TRG0_0, ADC0_TRG0_1	-	$5t_{CLK_LCP1A}$	-	ns	$5t_{CLK_LCP1A}$

7.4.11 Low Voltage Detection (External Voltage)

7.4.11.1 Low-voltage Detection (external low-voltage detection for LVDH1)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Guaranteed MCU operation range	Remarks
				Min	Typ	Max			
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b000	2.41	2.5	2.59	V	No	*1
Release voltage	V_{DLAT}	V_{CC5}		2.51	2.6	2.69	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b001	2.7	2.8	2.9	V	Yes	-
Release voltage	V_{DLAT}	V_{CC5}		2.8	2.9	3.0	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b010	3.47	3.6	3.73	V		
Release voltage	V_{DLAT}	V_{CC5}		2.57	3.7	3.83	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b011	3.67	3.8	3.93	V		
Release voltage	V_{DLAT}	V_{CC5}		3.76	3.9	4.04	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b100	3.86	4	4.14	V		
Release voltage	V_{DLAT}	V_{CC5}		3.96	4.1	4.24	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b101	4.05	4.2	4.35	V		
Release voltage	V_{DLAT}	V_{CC5}		4.15	4.3	4.45	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b110	2.61	2.7	2.79	V	No	*1
Release voltage	V_{DLAT}	V_{CC5}		2.7	2.8	2.9	V		
Detection voltage	V_{DLAT}	V_{CC5}	LVDH1V=0b111 (Initial value)	2.51	2.6	2.69	V		
Release voltage	V_{DLAT}	V_{CC5}		2.61	2.7	2.79	V		
Low-voltage detection/release time	T_d	-	-	-	-	40		-	*2
Power supply voltage regulation	-	V_{CC5}	-	-2	-				

7.4.11.2 Low-voltage Detection (external low-voltage detection for LVDH2)

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Guaranteed MCU operation range	Remarks
				Min	Typ	Max			
Detection voltage	V_{DLAT53}	V_{CC53_1}	LVDH2V=0b0001 (Initial value)	2.7	2.8	2.9	V		
Release voltage	V_{DLAT53}	V_{CC53_1}		2.8				Yes	-

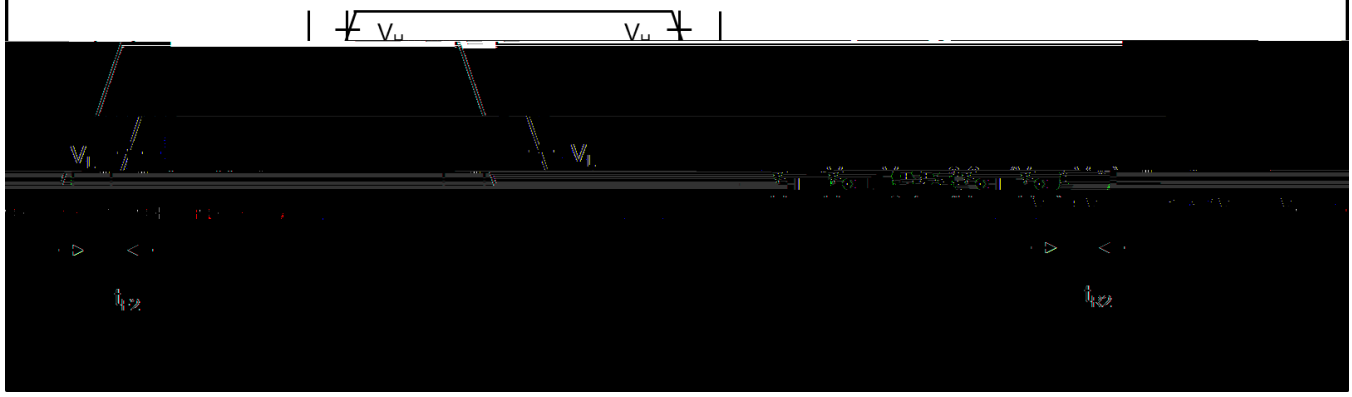
7.4.13 High Current Output Slew Rate

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise / fall time	t_{R2}, t_{F2}	GPIO of DV_{CC}*1	-	15	-	100	ns	Load capacitance 85pF

*1: For the details of GPIO group, refer to section 5.3
When I/O output drive capacity setting is 30 mA.

・Slew rate output timing



7.4.14 External bus interface timing

7.4.14.1 Clock output timing

(T_A: Recommended operating conditions, V_{cc53_1}=5.0 V ±10%, V_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	MCLK		25	-	ns	
Clock high width *1	t_{CHCL}	MCLK	(C_L=20pF, I_{OH}=-5mA, I_{OL}=5mA)	d_Ht_{CYC}-4.5	d_Ht_{CYC}+4.5		

7.4.14.2 Common timing between read and write

(T_A: Recommended operating conditions, V_{cc53_1}=5.0 V ±10%, V_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time (without MRDY)	t_{CYC}	MCLK	(C_L= 20 pF, I_{OH}= -5 mA, I_{OL}=5 mA)	25	-	ns	
Cycle time (with MRDY)	t_{CYC}	MCLK		40	-	ns	If using MRDY, set MCLK to 25 MHz or less.
CS delay time	t_{CSO}	MCLK, MCSX0 to MCSX3		0.5	11.25	ns	
Address delay time	t_{AO}	MCLK, MAD0 to MAD21		0.5	11.25	ns	
RDY setup time	t_{RDYS}	MCLK, MRDY	"CMOS hysteresis input" and "Disable noise filter" are selected.	21	-	ns	
RDY hold time	t_{RDYH}	MCLK, MRDY		0	-	ns	

7.4.14.3 Read timing

(T_A: Recommended operating conditions, V_{cc53_1}=5.0 V ±10%, V_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data setup time	t_{DSR}	MOEX, MDATA0 to MDATA15					

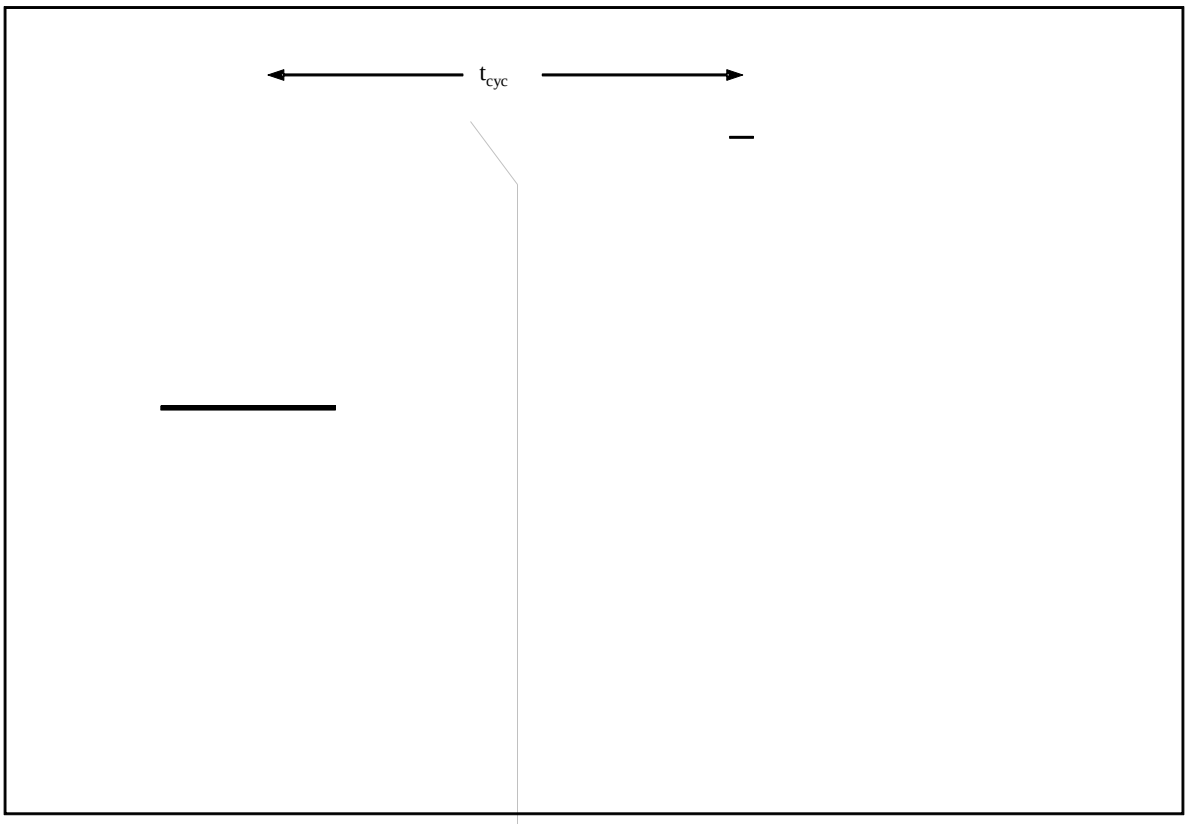
7.4.14.4 Write timing

(T_A: Recommended operating conditions, V_{cc53_1}=5.0 V ±10%, V_{SS}=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MWEX delay time	t_{WEO}	MCLK, MWEX	(C_L=20 pF, I_{OH}= -5 mA, I_{OL}=5 mA)	0.5	11.25	ns	
Byte mask delay time	t_{WRO}	MCLK, MDQM0, MDQM1		0.5	11.25	ns	
Data delay time	t_{DO}	MCLK, MDATA0 to MDAT15		0.5	11.25	ns	
Data delay time (Hi-Z output)	t_{DOZ}	MCLK, MDATA0 to MDAT15		-	11.25	ns	

Notes: This is target spec.

External bus I/F write timing

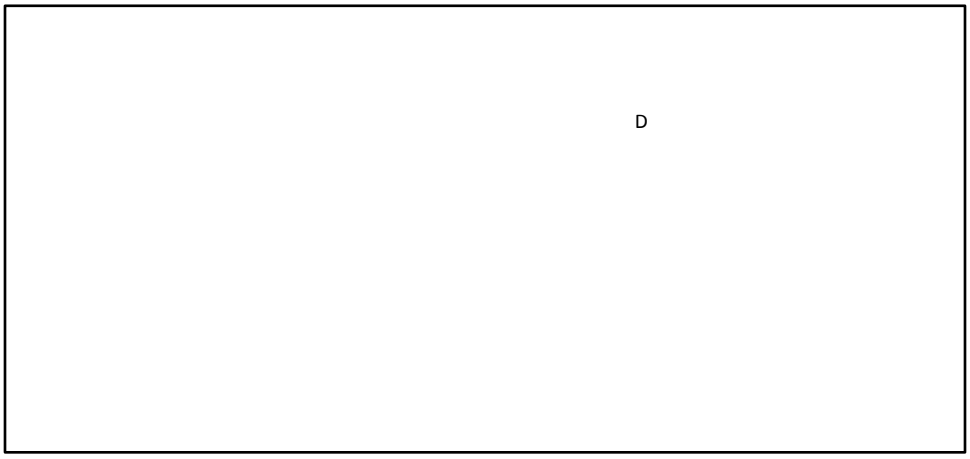

t_{cyc}

(2) DDR-

7.4.18 LCD Bus I/F

(Condition: See Section 7.2 Recommended Operating Conditions)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock cycle time	t_{CLK}	WR#, RD#	(CL = 20 pF, I_{OL}= -5 mA, I_{OH}= 5 mA),	25	-	ns	
Signal-to-Signal uncertainty	t_{UNCERT}	CS#		-	5.0	ns	
Output to input duration	t_{OUT2IN}	LCDD0 to LCDD17		-	28.0	ns	



Note:

- *To calculate interface timing, refer to the LCD controller specification of the external display for the required AC characteristics and S6J3360/S6J3370 Series hardware manual.*

(T_A: Recommended operating conditions, V_{CC}= AV_{CC5}=3.3 V ± 0.3 V, V_{SS}=AV_{SS}=0.0 V)

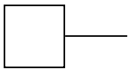
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total Error	-	-	-	-	±6		

7.5.2 Notes on A/D Converters

Output impedance of an external circuit for analog input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model



	R	C		
12-bit A/D	3 k (max)	7.8 pF (max)		AV_{CC5} 5 V)
12-bit A/D	6 k (max)	7.8 pF (max)	(3.0	V_{CC5} 5 V)

Note: Use the numerical values provided here simply as a guide.

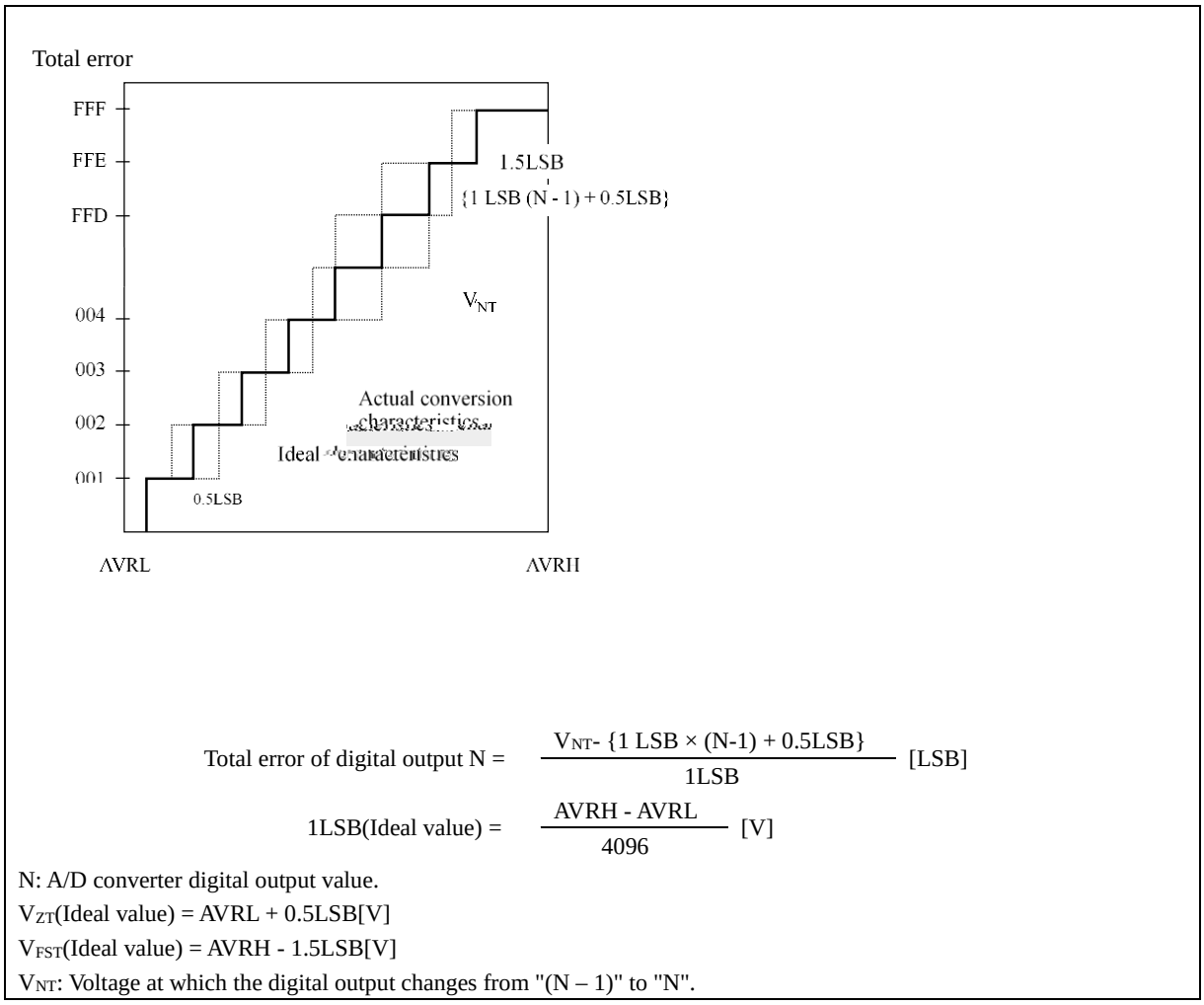
7.5.3 Glossary

Resolution: Analog change that can be identified by an A/D converter.

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB.

Total error: Difference between the actual value and the theoretical value.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\text{LSB}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB(Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{4096}\ [\text{V}]$$

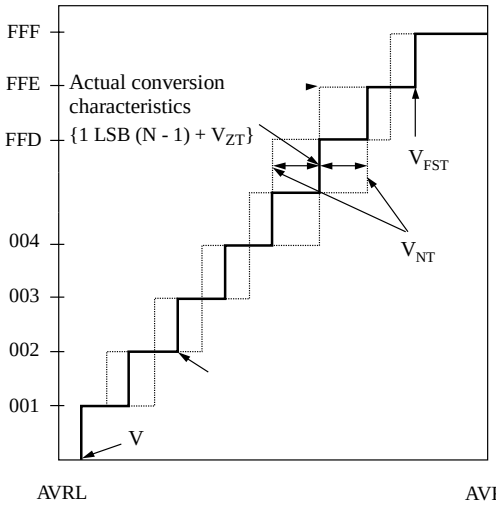
N: A/D converter digital output value.

V_{ZT}(Ideal value) = AVRL + 0.5LSB[V]

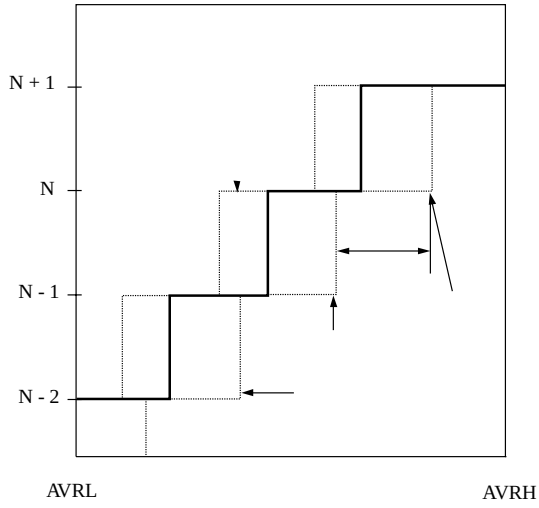
V_{FST}(Ideal value) = AVRH - 1.5LSB[V]

V_{NT}: Voltage at which the digital output changes from "(N – 1)" to "N".

Integral linearity error



Differential linearity error



$$\text{Integral linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

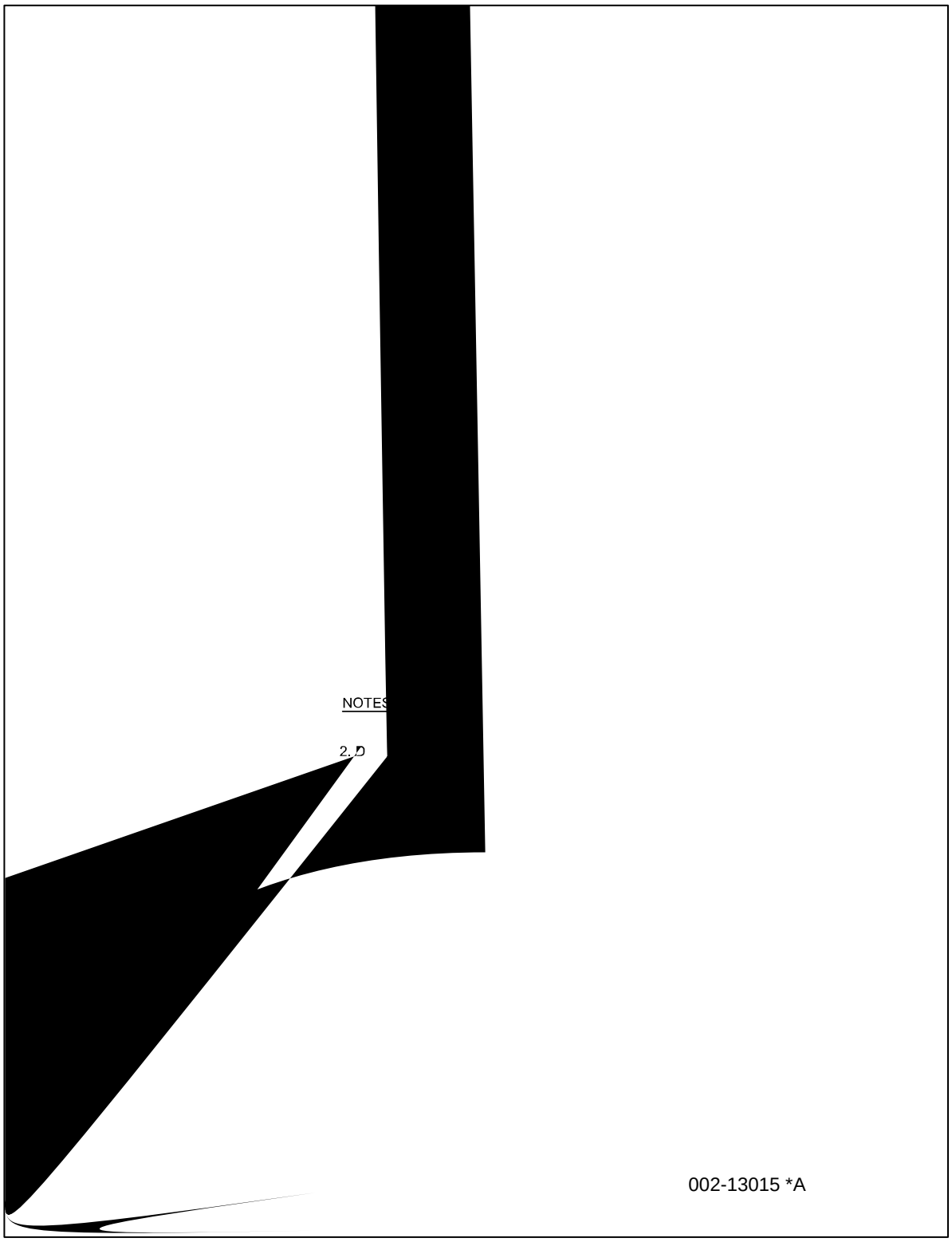
V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

9.

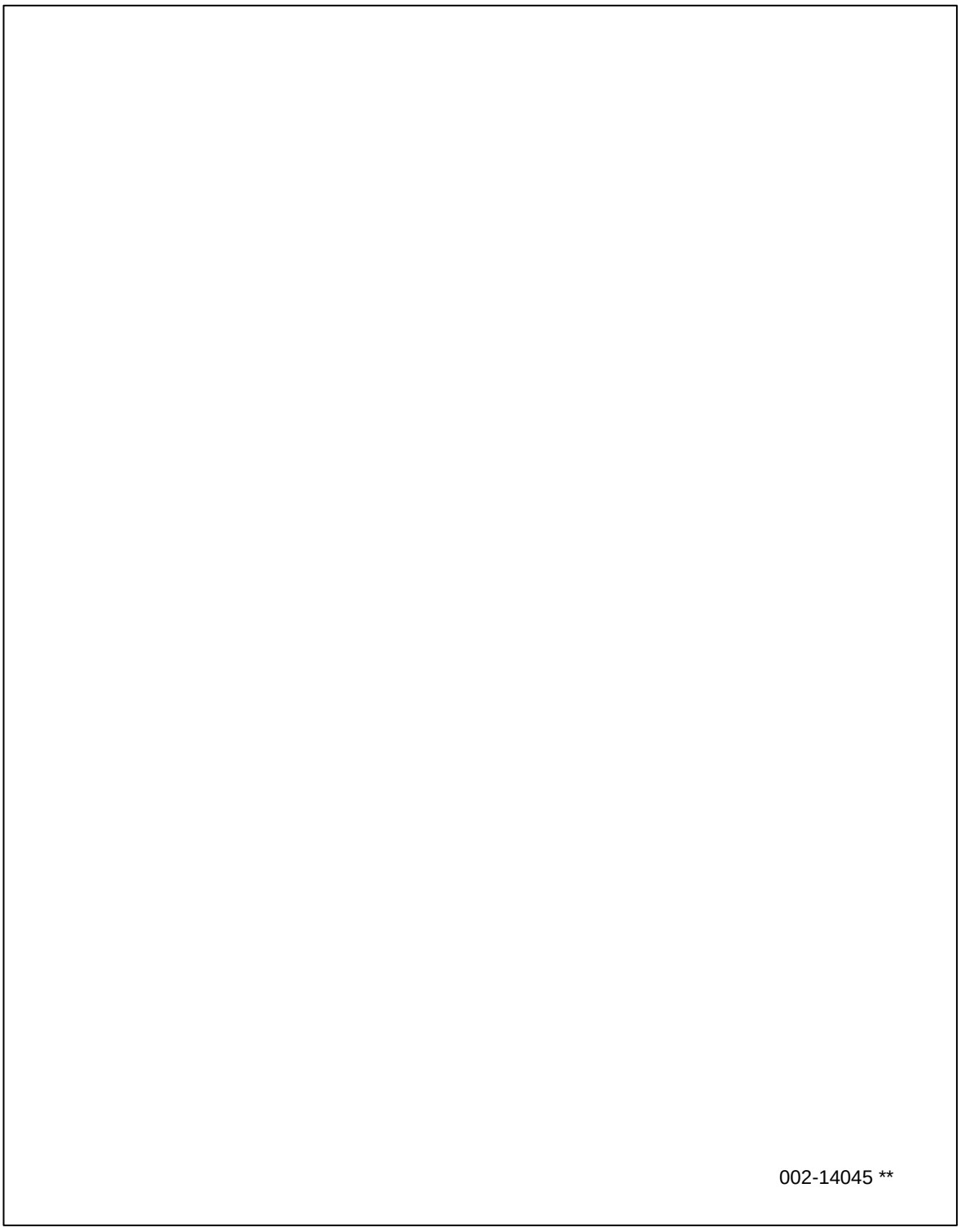
9.2 LQFP144 (0.5 mm)

Package Type	Package Code
LQFP 144	LQS 144



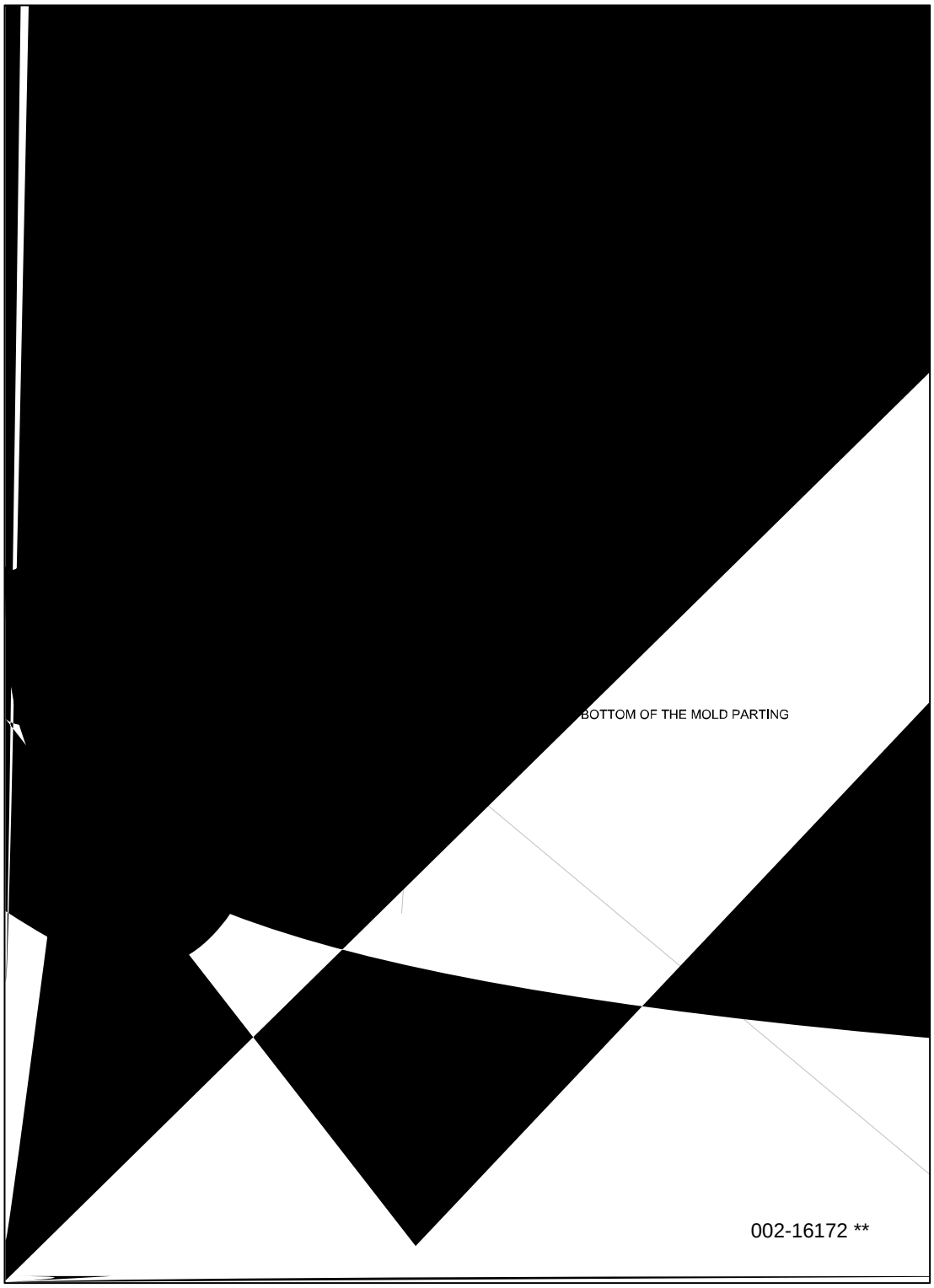
9.3 LQFP144 (0.4 mm)

Package Type	Package Code
LQFP 144	LQN 144



9.4 LQFP120

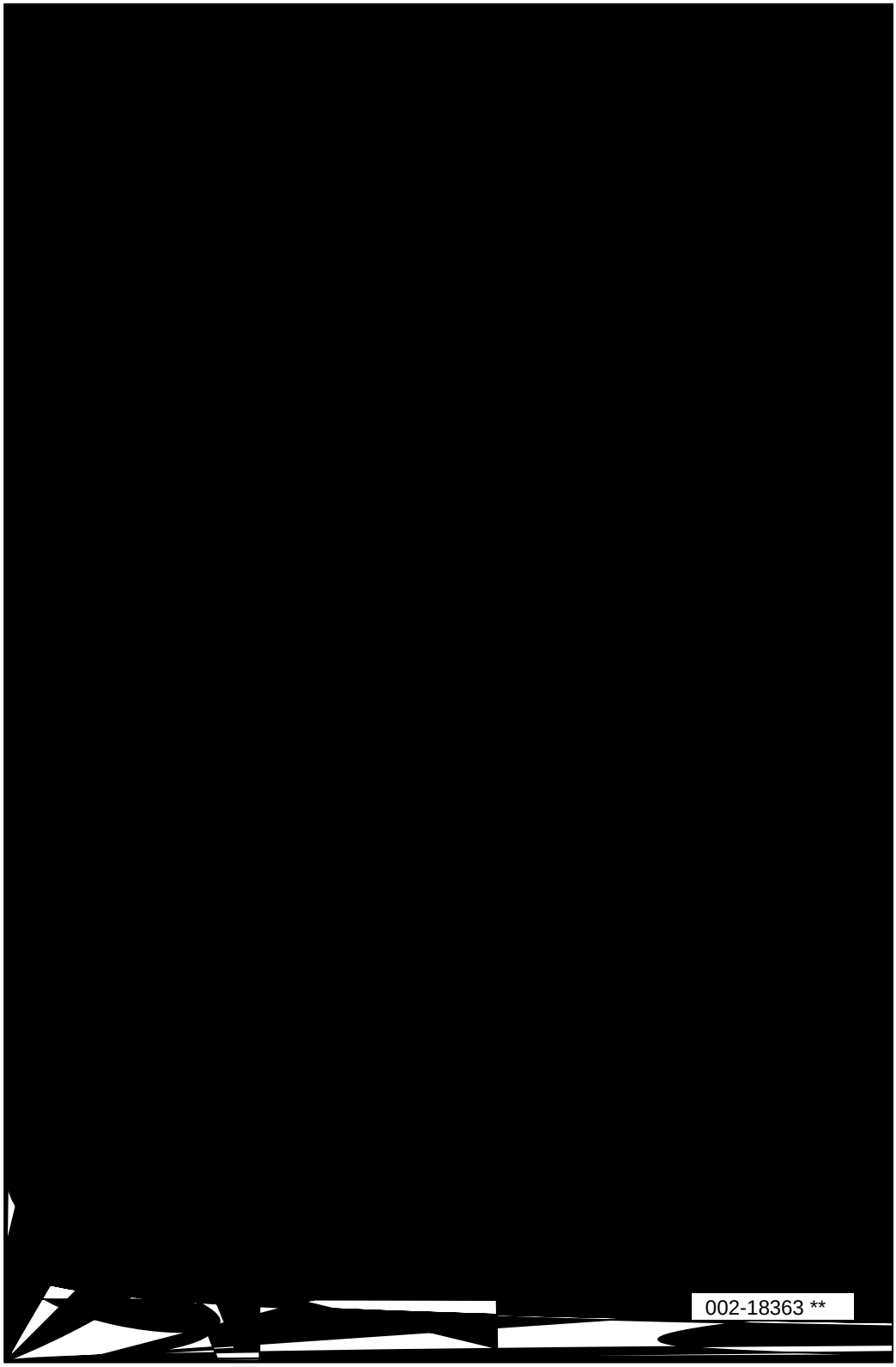
Package Type	Package Code
LQFP 120	LQM 120



9.5 LQFP100

9.6 TEQFP176

Package Type	Package Code
TEQFP 176	LEF176



9.7 TEQFP144 (0.5 mm)

Package Type	Package Code
TEQFP 144	LEJ 144

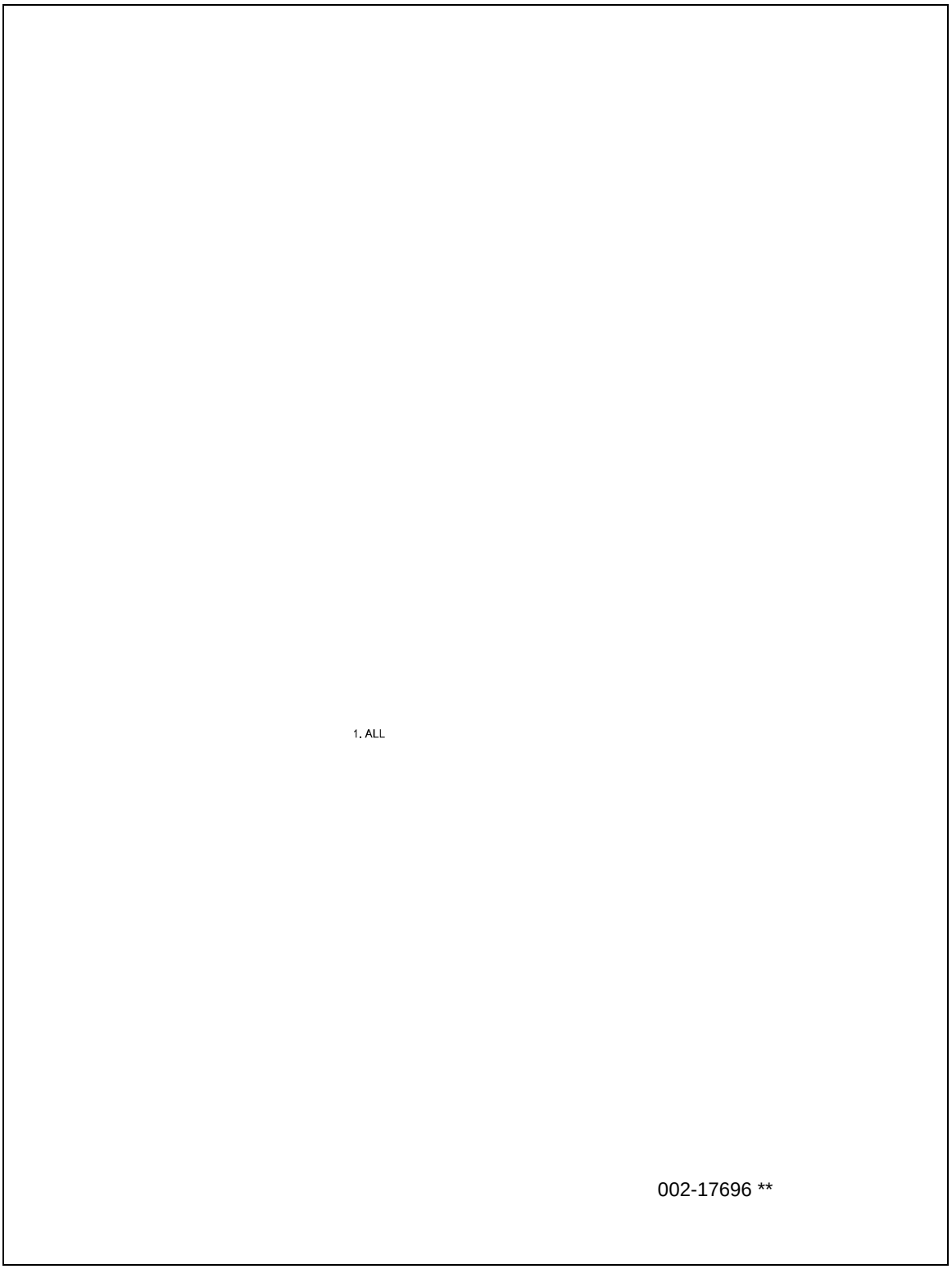
SYMBOL			
	MIN.	NOM.	MAX.
A	—	—	1.70
A 1	0.05	—	0.15
D	22.00 BSC		
D 1	20.00 BSC		
D 2	5.00 REF		
D 3	3.80 REF		
E	22.00 BSC		
E 1	20.00 BSC		
E 2	5.00 REF		
E 3	3.80 REF		
R 2	0.08	—	0.20
	0°	4°	8°
c	0.12	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L 1	1.00 REF		

2. DATUM PLANE H IS LOCATE

002-13036 *A

9.8 TEQFP144 (0.4 mm)

Package Type	Package Code
TEQFP 144	LEG 144



9.10 TEQFP100

Package Type	Package Code
TEQFP 100	LEI 100

10. Acronyms

Acronym	Definition
A/D converter	Analog digital converter
ADC	Analog-to-digital converter
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
AXI	Advanced extensible interface
BT	Base timer
CAN	Controller area network
CAN FD	Controller area network with flexible dap.74 5(rk)·

Acronym	Definition
LCDC	LCD controller
LCD_IF	LCD bus interface
LIN	local interconnect network
LVD	Low-voltage detector
MCU	Microcontroller unit
MFS	Multi-function serial interface

MPU

11. Appendix

11.1

This is an application example of JTAG tool connection with 120-pin PKG.

This is an application example of JTAG tool connection with 100-pin PKG.

Document History

Document Title:

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Corrected I2S Communication Port 1 WS_0 I2S1_SCK_0

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB ConC>9<0aoll95(e)-3((s)] TJETBT1 0 0 1 1 9.46 472.39 Tm[( )] TJETBT1 0 0 1 280.81 472.39 Tm0.133 0.345 0.69 rg0.133 0.345 0.69 R	

irle93(s)-6(s7(/RFe)] TJETBT1 0 0 1 14.446 568.35 Tm[( )] TJETBT1 0 0 1 200.81 568.35 Tm0.133 0.345 0.69 rg0.133 0.345 0.69 RG[(c)-6(y)