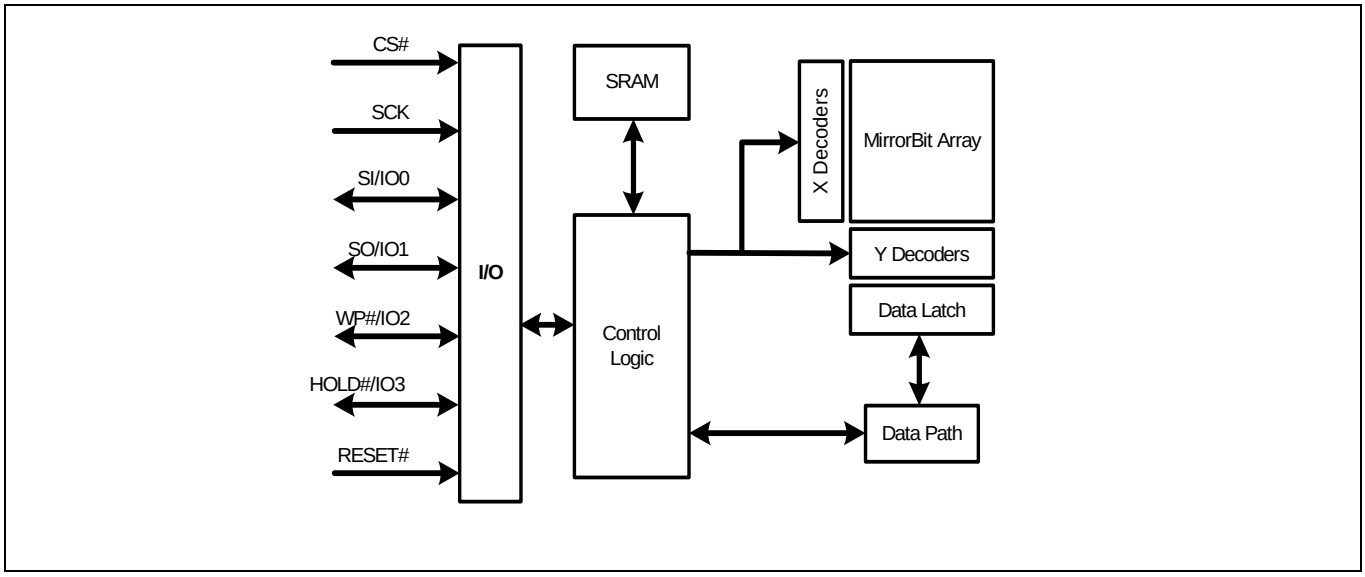
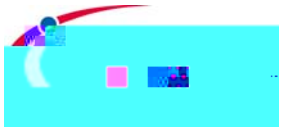
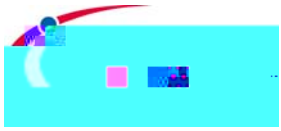
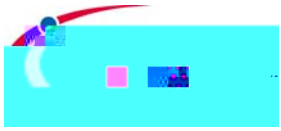
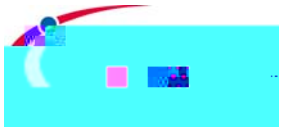


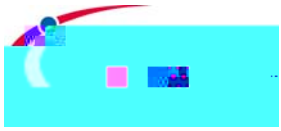

CS#
SCK
SI/IO0
SO/IO1
WP#/IO2
HOLD#/IO3
RESET#
I/O
SRAM
Control Logic
X Decoders
MirrorBit Array
Y Decoders
Data Latch
Data Path





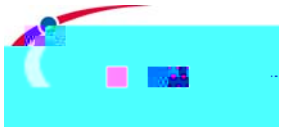


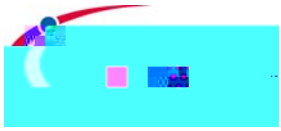


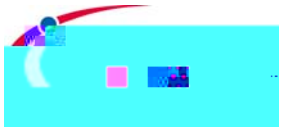


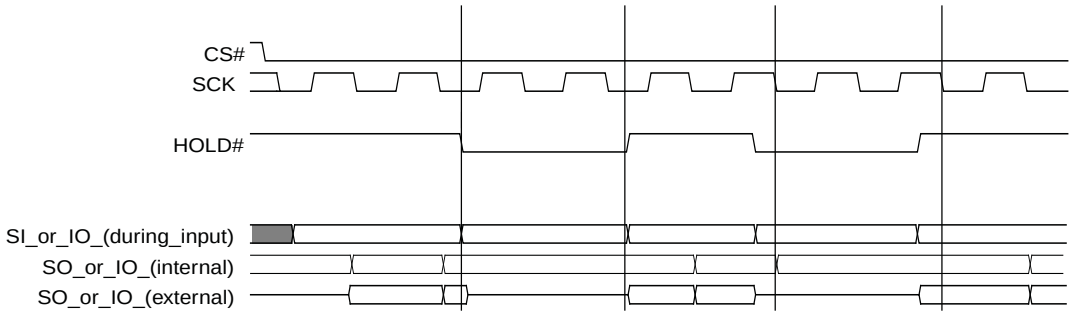


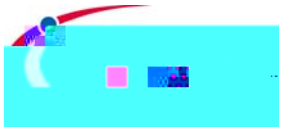
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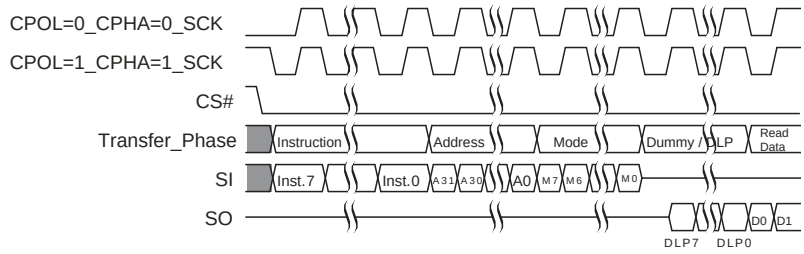


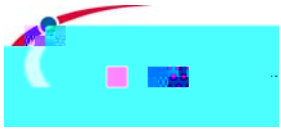


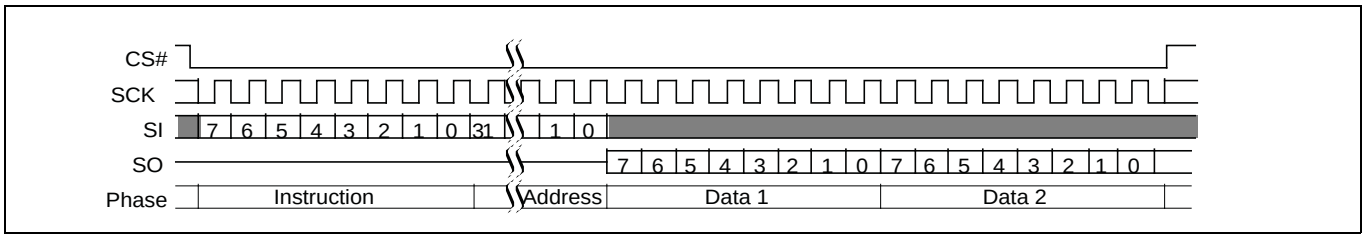


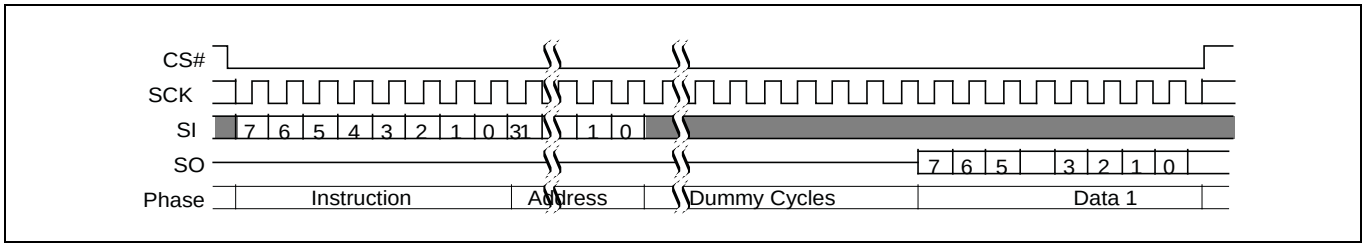

CS#
SCK
HOLD#
SI_or_IO_(during_input)
SO_or_IO_(internal)
SO_or_IO_(external)

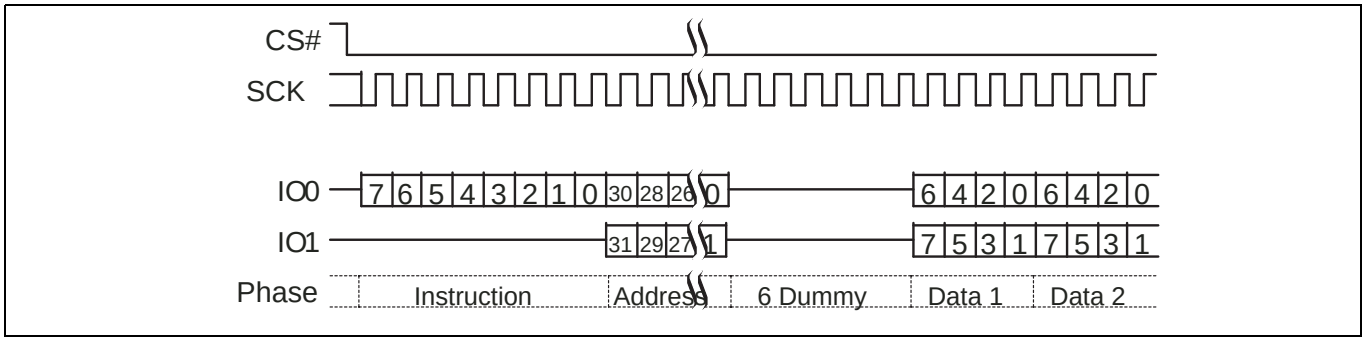


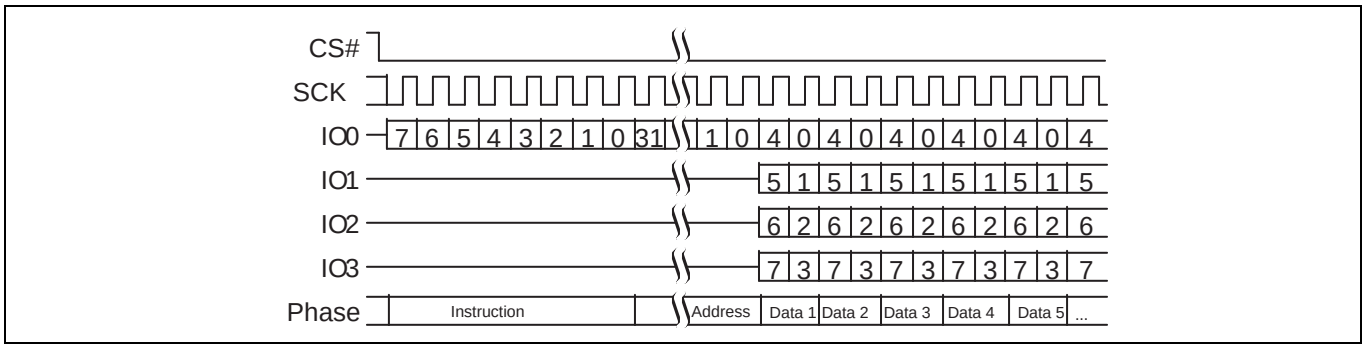

CPOL=0_CPHA=0_SCK
CPOL=1_CPHA=1_SCK
CS#
Transfer_Phase
SI
SO
Instruction
Address
Mode
Dummy / DLP
Read Data
Inst.7
Inst.0
A31
A30
A0
M7
M6
M0
D0
D1
DLP7
DLP0

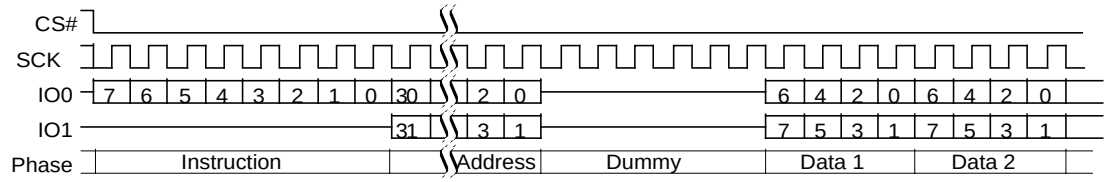


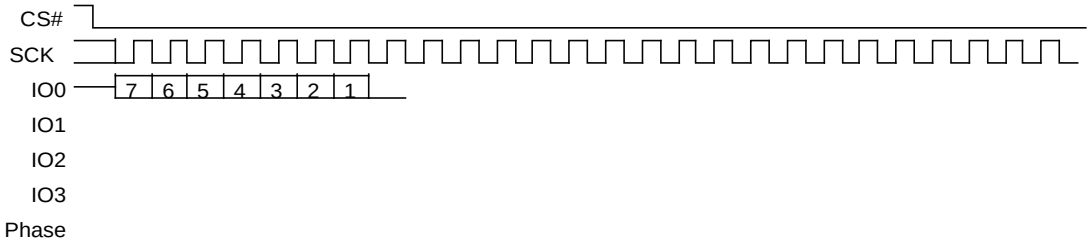

CS#
SCK
SI
SO
Phase
Instruction
Address
Data 1
Data 2

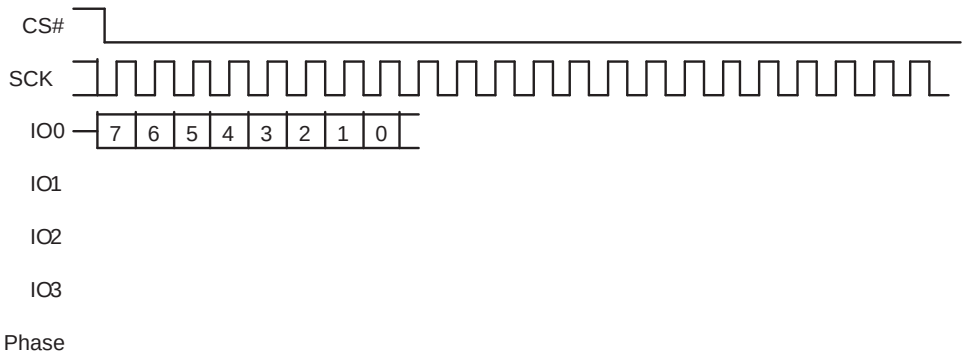

CS#
SCK
SI
SO
Phase
Instruction
Address
Dummy Cycles
Data 1


CS#
SCK
IO0
IO1
Phase
Instruction
Address
6 Dummy
Data 1
Data 2


CS#
SCK
IO0
IO1
IO2
IO3
Phase
Instruction
Address
Data 1
Data 2
Data 3
Data 4
Data 5
...

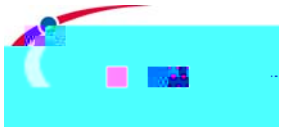

CS#
SCK
IO0
IO1
Phase
7 6 5 4 3 2 1 0 30 2 0 6 4 2 0 6 4 2 0
31 3 1 7 5 3 1 7 5 3 1
Instruction
Address
Dummy
Data 1
Data 2

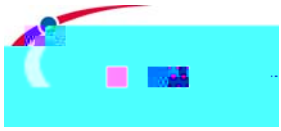

CS#
SCK
IO0
IO1
IO2
IO3
Phase
7 6 5 4 3 2 1

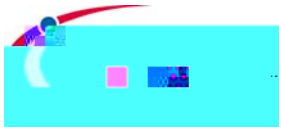

CS#
SCK
IO0
7
6
5
4
3
2
1
0
IO1
IO2
IO3
Phase

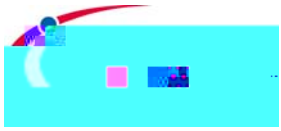
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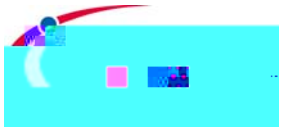
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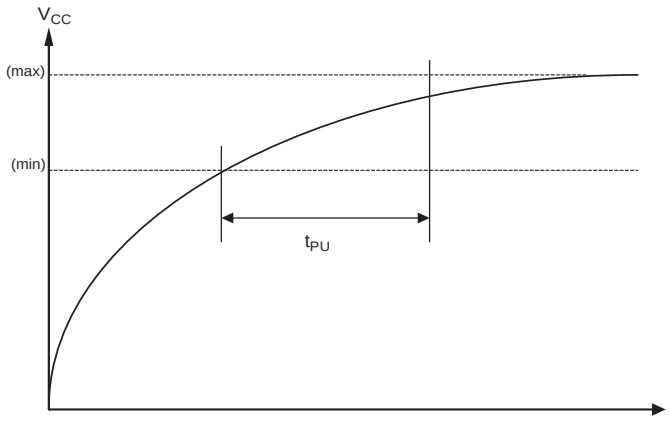


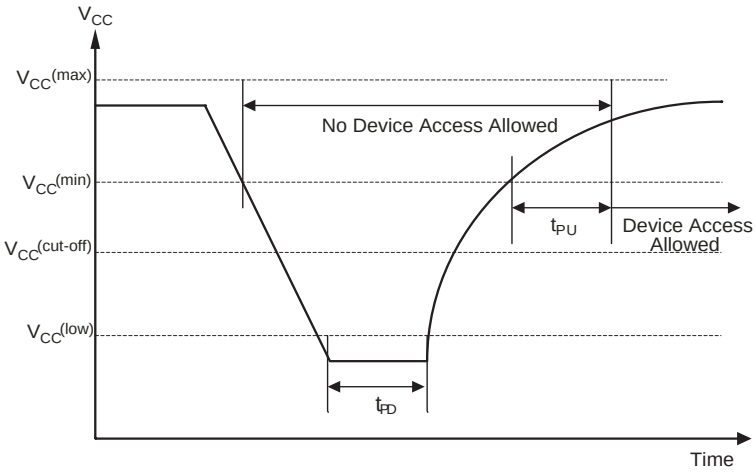


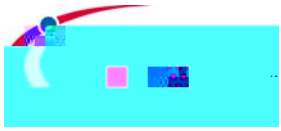


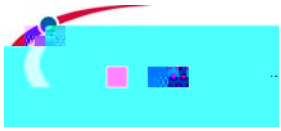


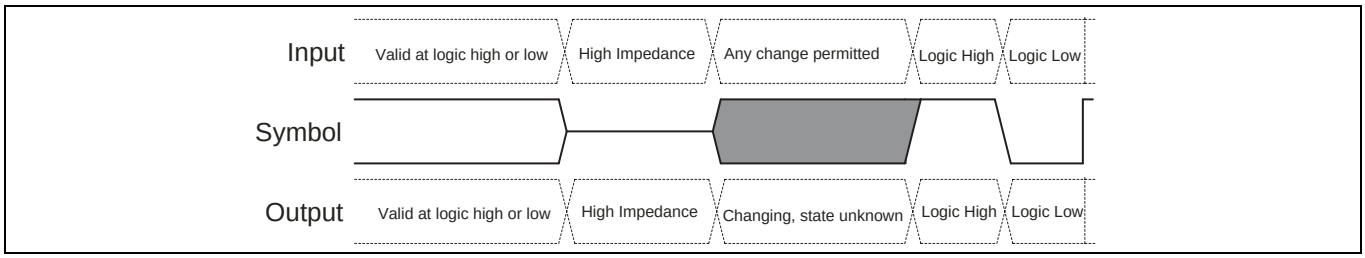
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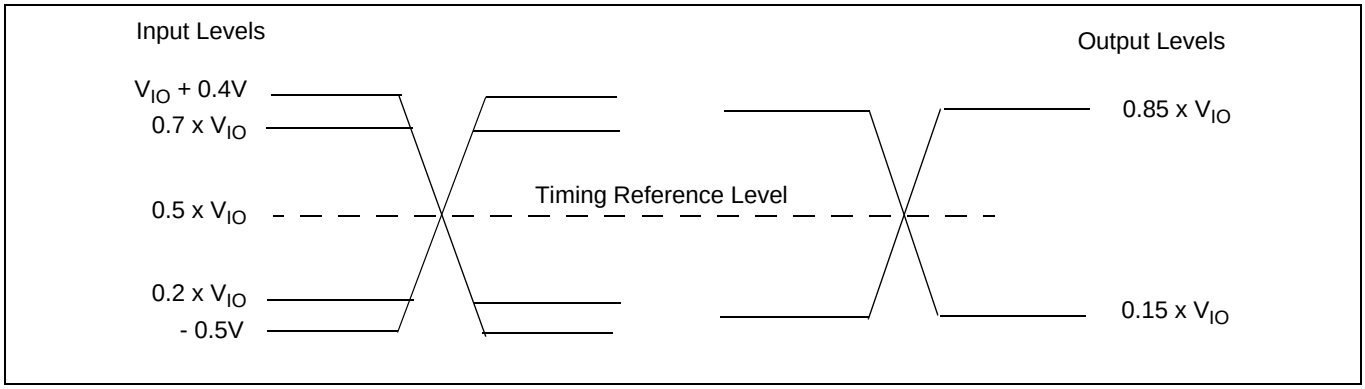


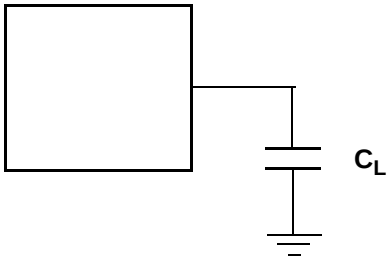

V_{CC}
$V_{CC}(max)$
$V_{CC}(min)$
$V_{CC}(cut\text{-}off)$
$V_{CC}(low)$
No Device Access Allowed
t_{PU}
Device Access Allowed
t_{PD}
Time

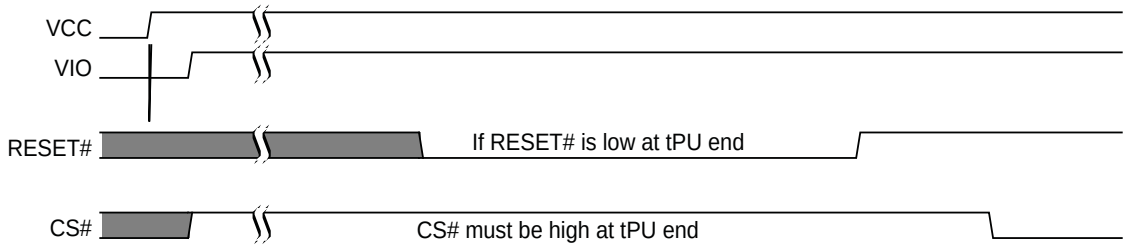


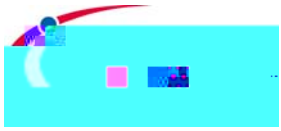



Input
Valid at logic high or low
High Impedance
Any change permitted
Logic High
Logic Low
Symbol
Output
Valid at logic high or low
High Impedance
Changing, state unknown
Logic High
Logic Low


Input Levels
Output Levels
V_{IO} + 0.4V
0.7 x V_{IO}
0.5 x V_{IO}
0.2 x V_{IO}
- 0.5V
Timing Reference Level
0.85 x V_{IO}
0.15 x V_{IO}


C_L

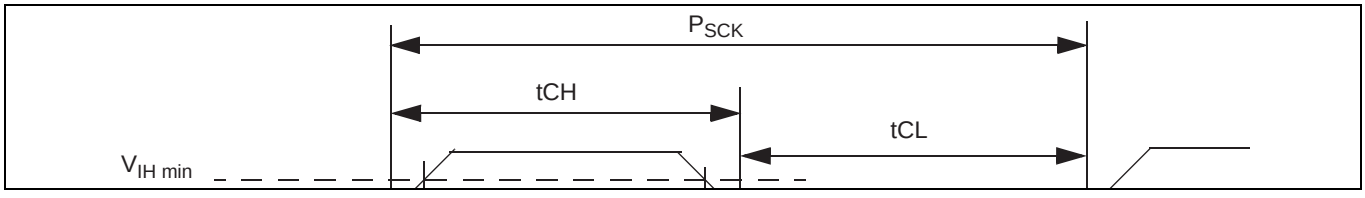

VCC
VIO
RESET#
If RESET# is low at tPU end
CS#
CS# must be high at tPU end



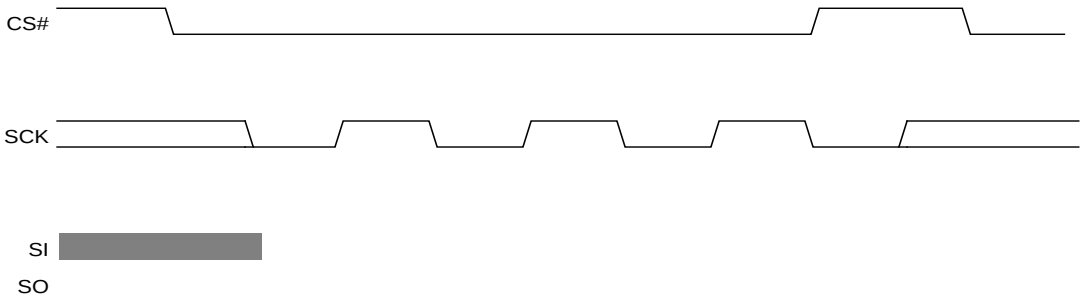
				∞	

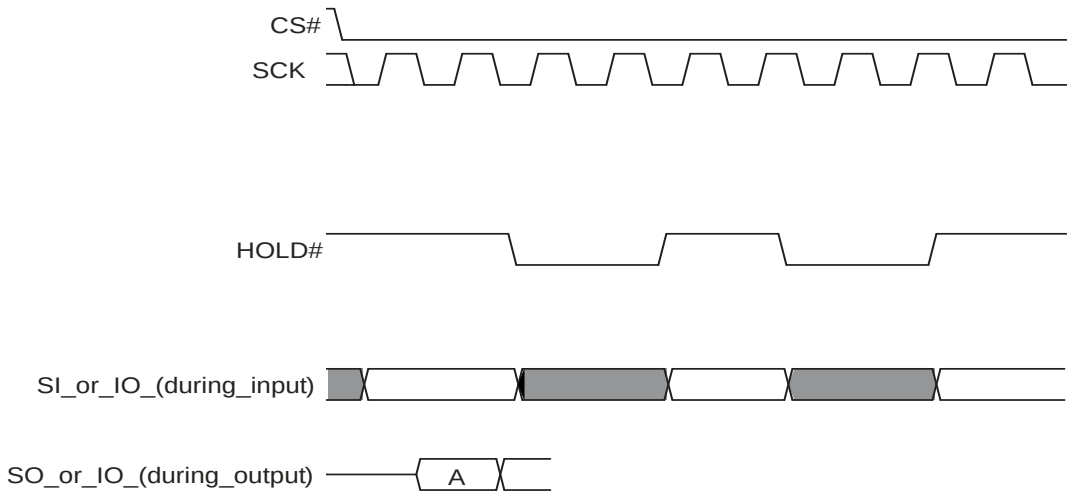
≤

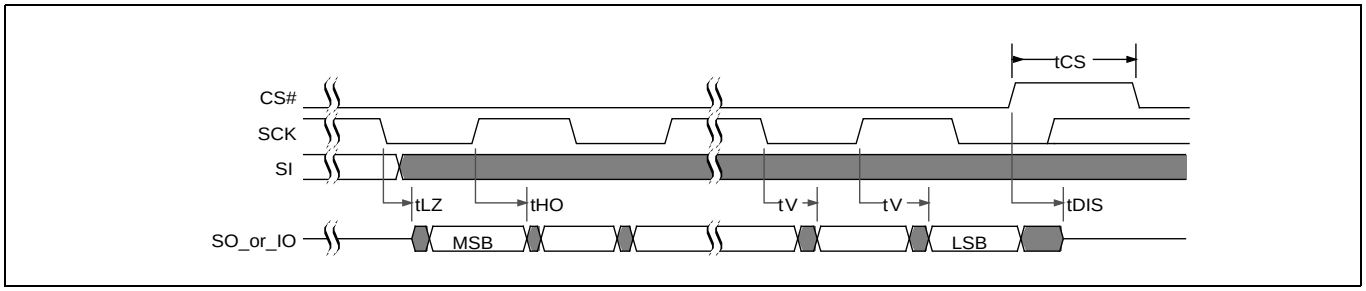
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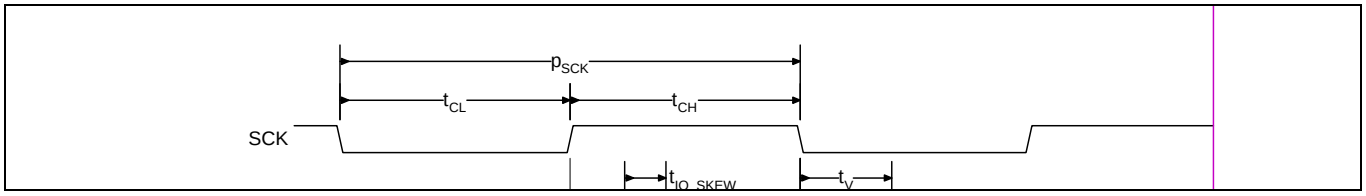

PSCK
tCH
tCL
VIH min

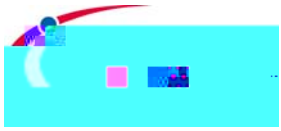
≤

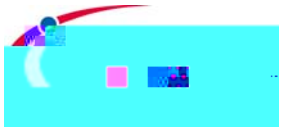

CS#
SCK
SI
SO

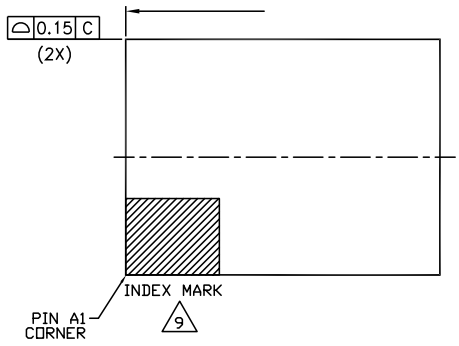

CS#
SCK
HOLD#
SI_or_IO_(during_input)
SO_or_IO_(during_output)
A

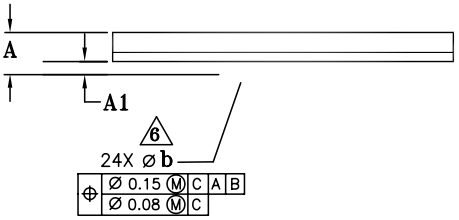

tCS
CS#
SCK
SI
tLZ
tHO
tV
tV
tDIS
SO_or_IO
MSB
LSB

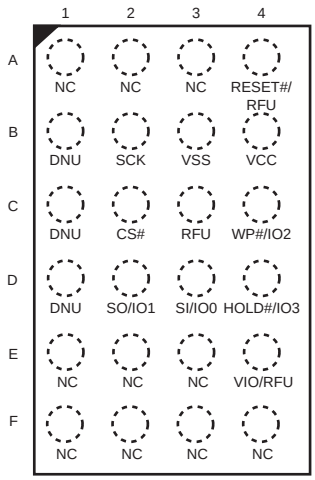

pSCK
tCL
tCH
SCK
tIO_SKEW
tV

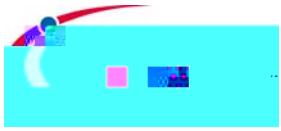


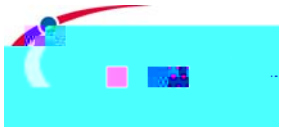


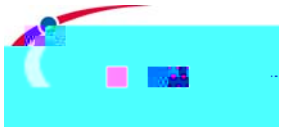

0.15 C
(2X)
INDEX MARK
9
PIN A1
CORNER

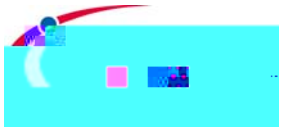

A
A1
6
24X ø b
Ø 0.15 M C A B
Ø 0.08 M C

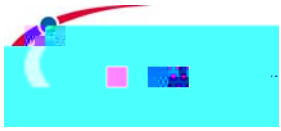

1 2 3 4
A
NC NC NC RESET#/ RFU
B
DNU SCK VSS VCC
C
DNU CS# RFU WP#/IO2
D
DNU SO/IO1 SI/IO0 HOLD#/IO3
E
NC NC NC VIO/RFU
F
NC NC NC NC

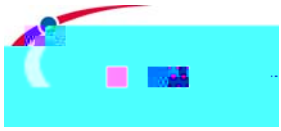


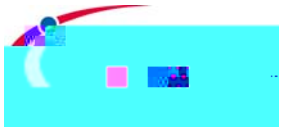


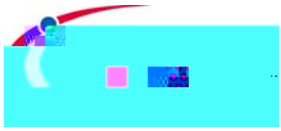


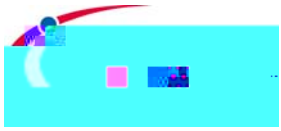


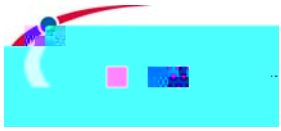


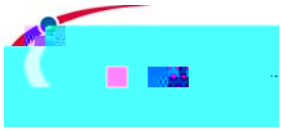


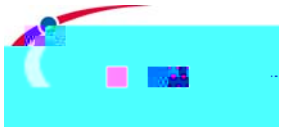


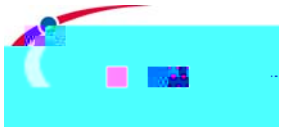


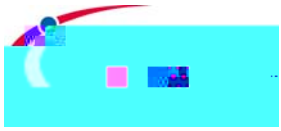


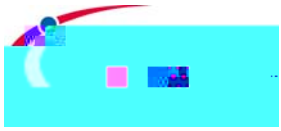


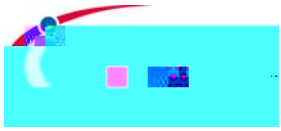


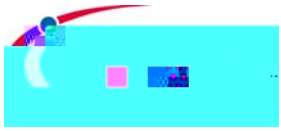


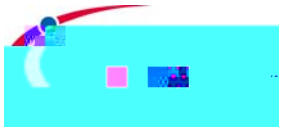


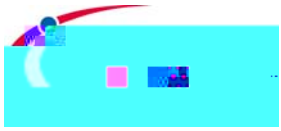


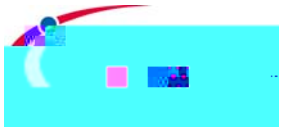


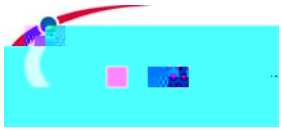


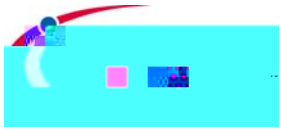


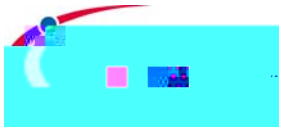


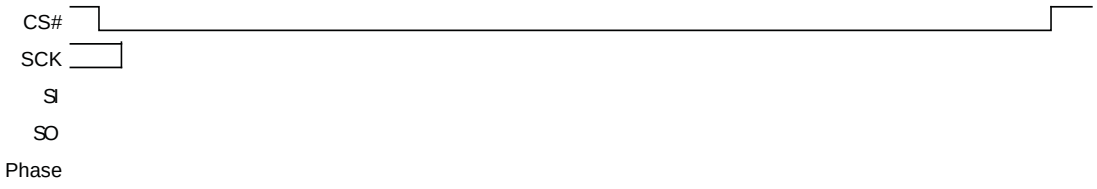


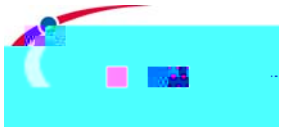


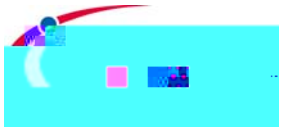


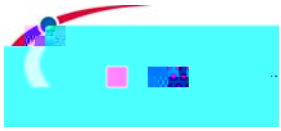


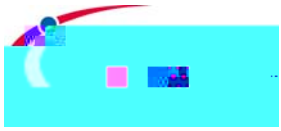


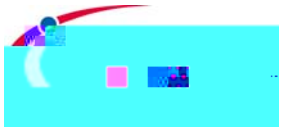

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SI
SO
Phase

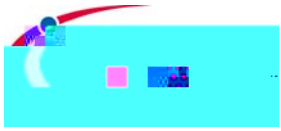


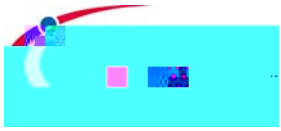


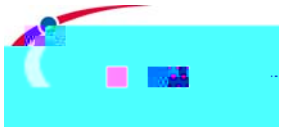


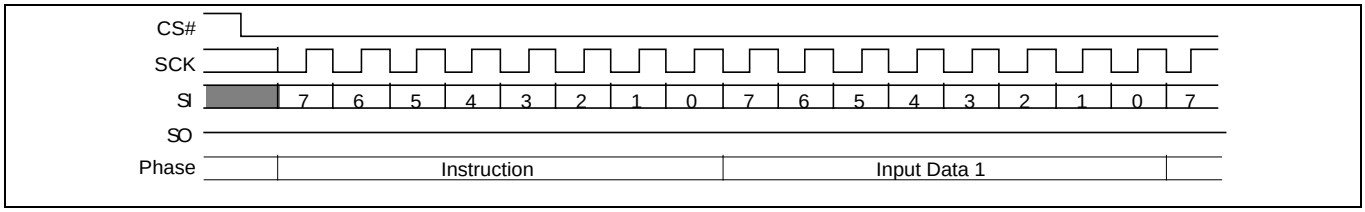


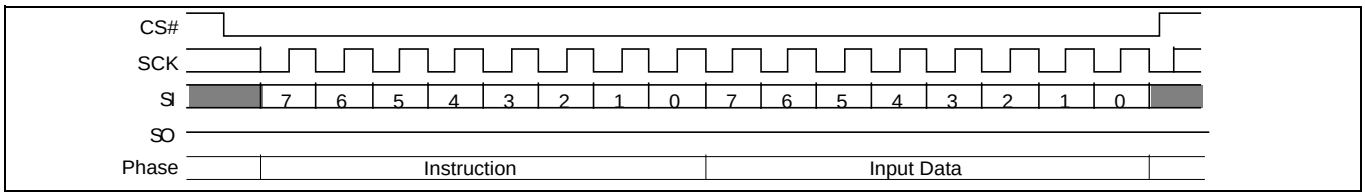


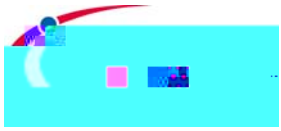


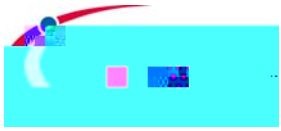


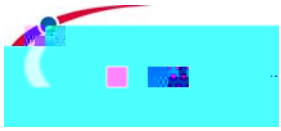


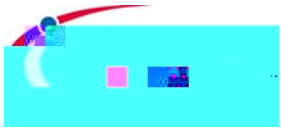

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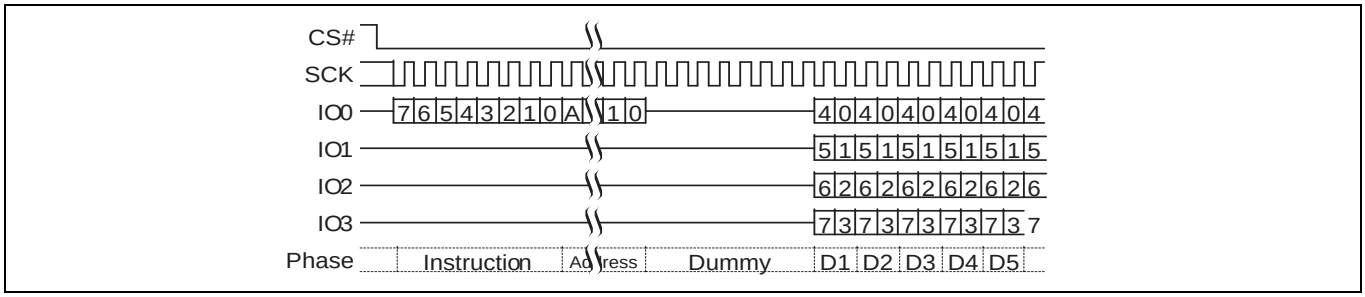

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SCK
SI
SO
Phase
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Instruction
Input Data

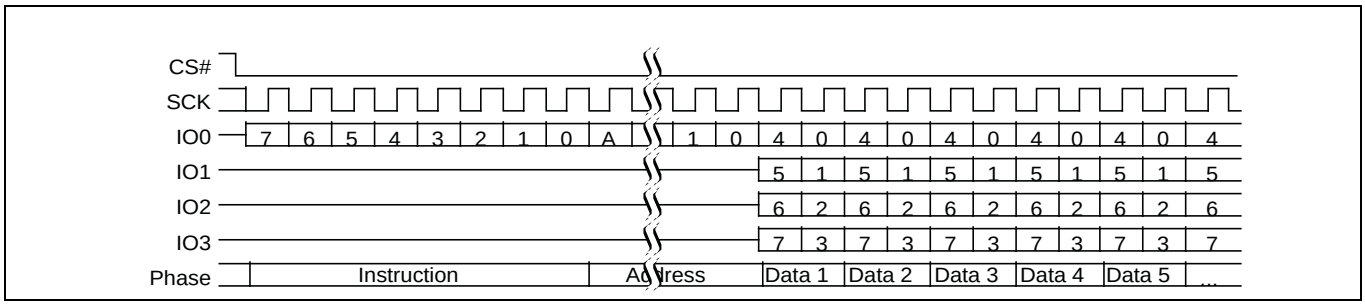


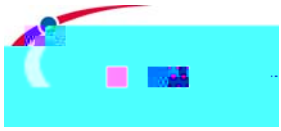


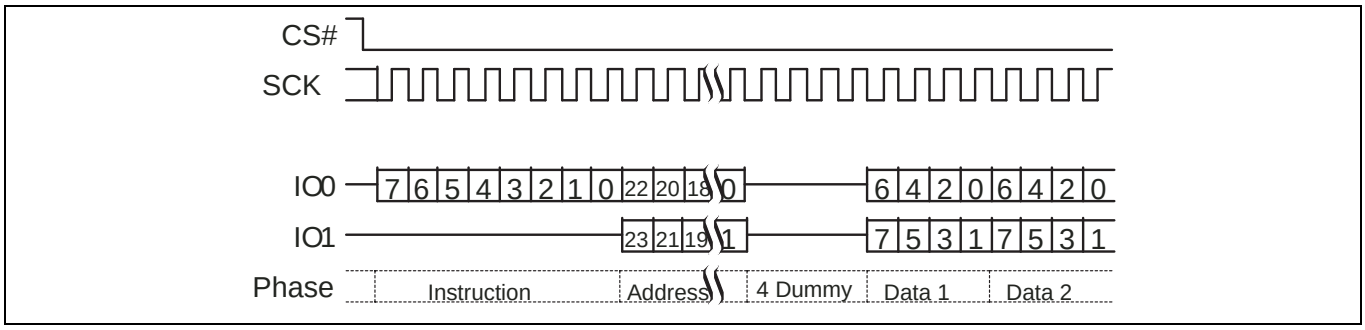


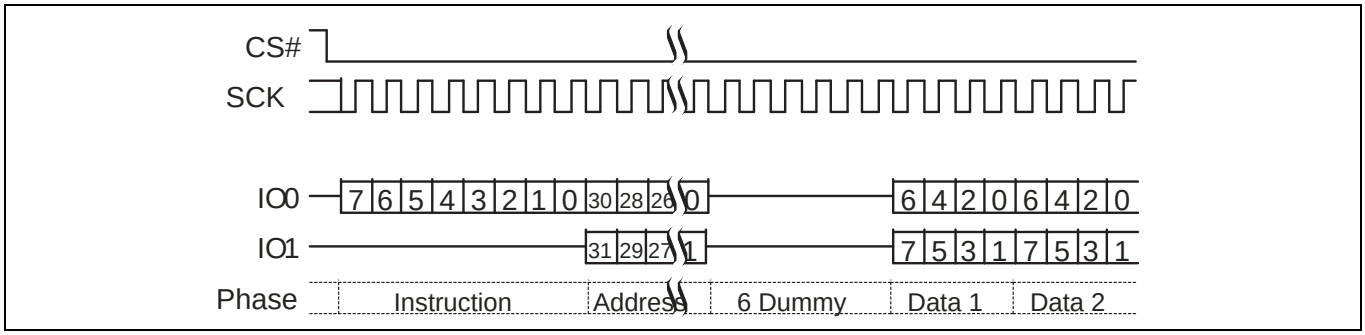


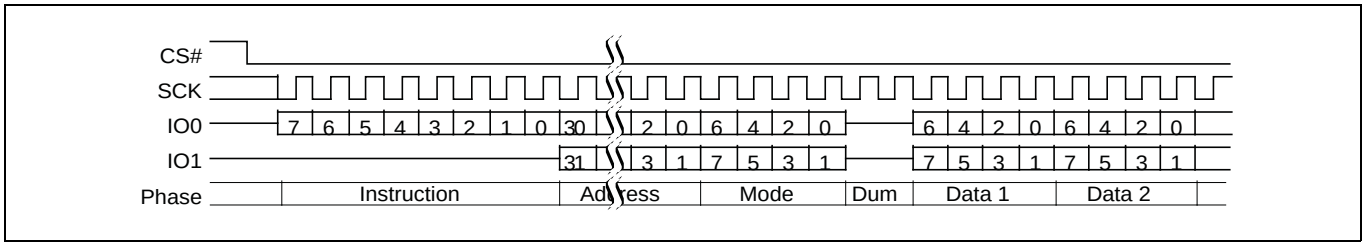

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IO1
IO2
IO3
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4 0 4 0 4 0 4 0 4 0 4
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Instruction
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Dummy
D1 D2 D3 D4 D5

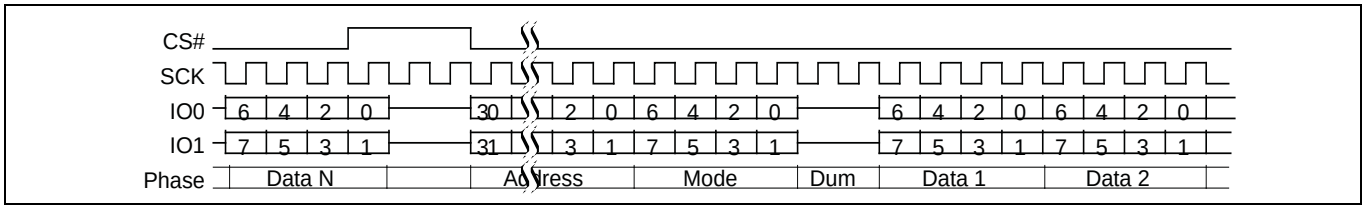

CS#
SCK
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IO1
IO2
IO3
Phase
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Instruction
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Data 1
Data 2
Data 3
Data 4
Data 5
...

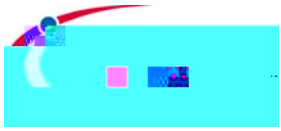


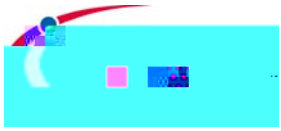

CS#
SCK
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IO1
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Instruction
Address
4 Dummy
Data 1
Data 2

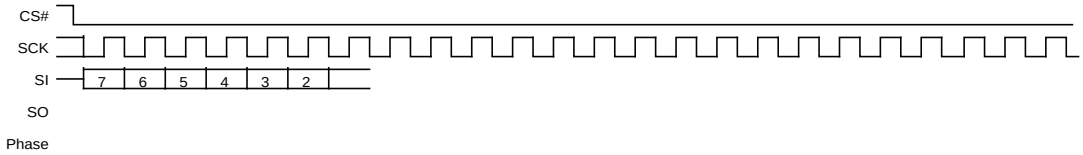

CS#
SCK
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IO1
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Instruction
Address
6 Dummy
Data 1
Data 2

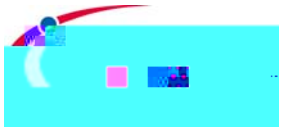

CS#
SCK
IO0
IO1
Phase
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Instruction
Address
Mode
Dum
Data 1
Data 2

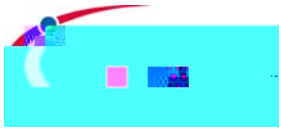

CS#
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IO1
Phase
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Data N
Address
Mode
Dum
Data 1
Data 2

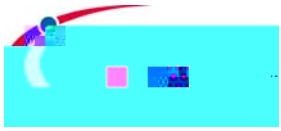


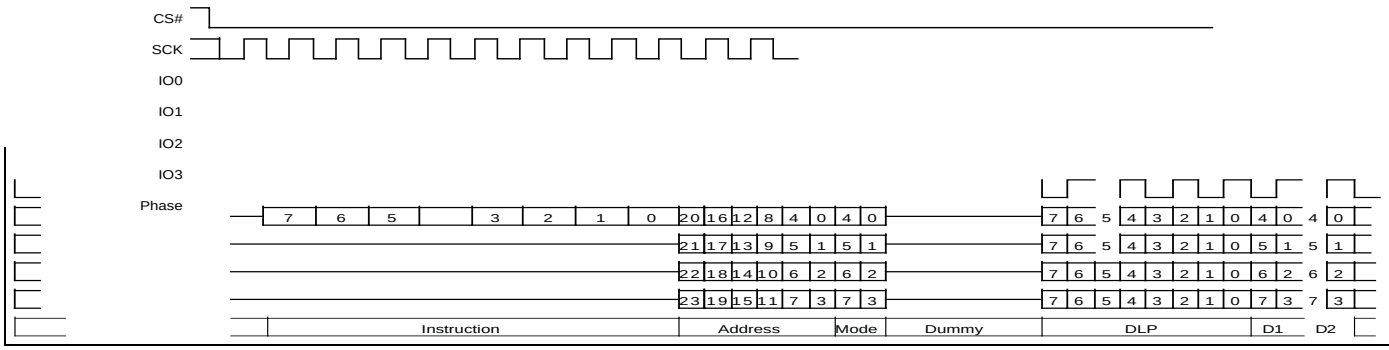


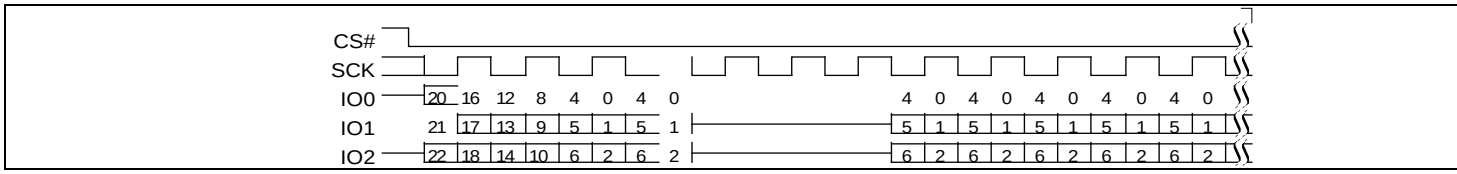

CS#
SCK
SI
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6
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3
2
SO
Phase

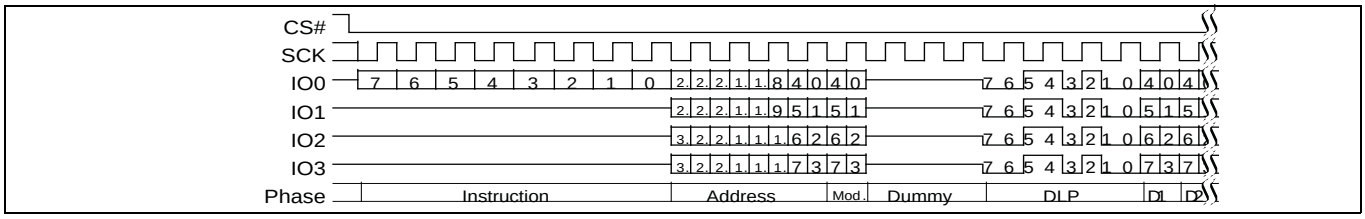


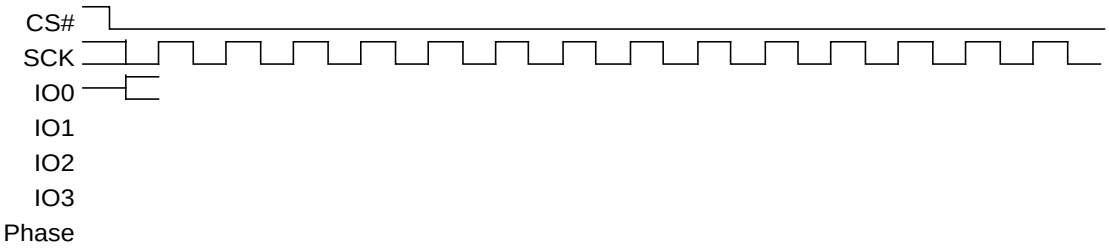


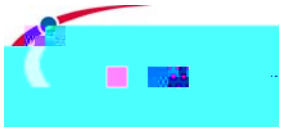


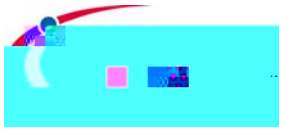

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SCK
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IO2
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Mode
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DLP
D1
D2

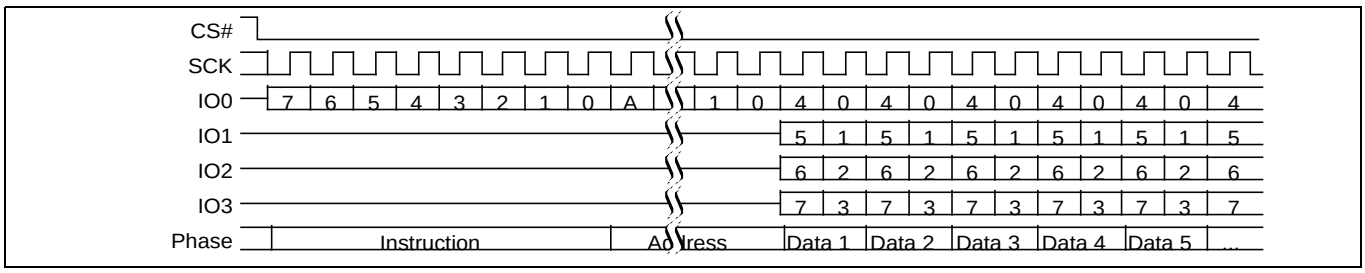

CS#
SCK
IO0
IO1
IO2

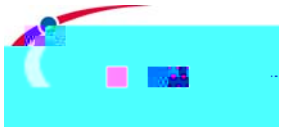

CS#
SCK
IO0
IO1
IO2
IO3
Phase
Instruction
Address
Mod.
Dummy
DLP
D1
D2

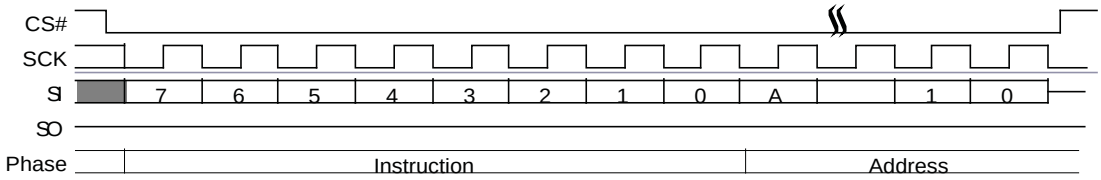

CS#
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IO0
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Phase

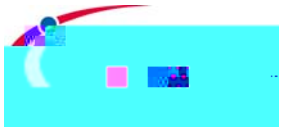


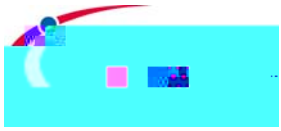


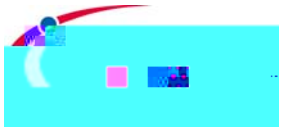

CS#
SCK
IO0
IO1
IO2
IO3
Phase
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Instruction
Address
Data 1
Data 2
Data 3
Data 4
Data 5
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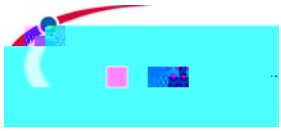


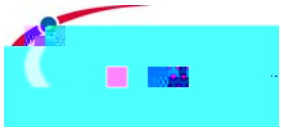

CS#
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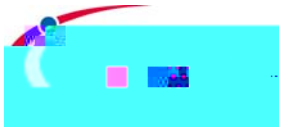


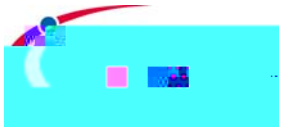


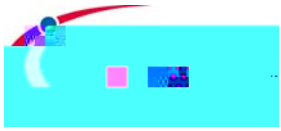


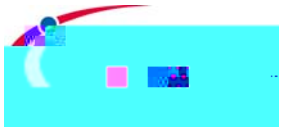


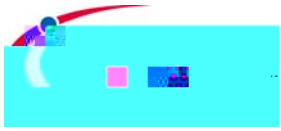

CS#
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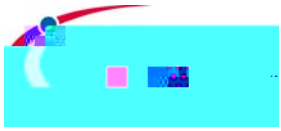


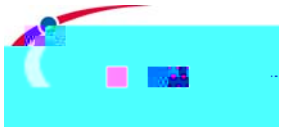




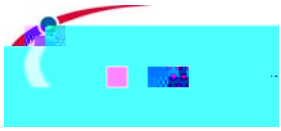




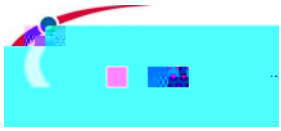


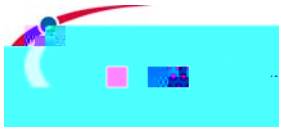


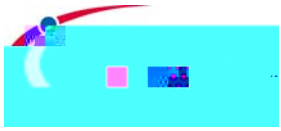
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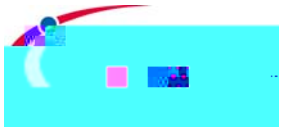


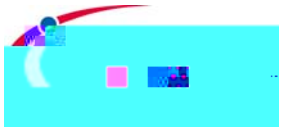
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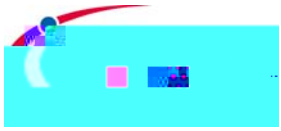




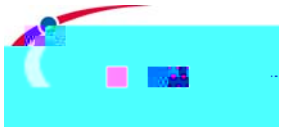


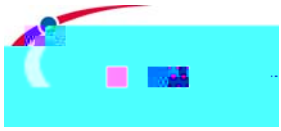


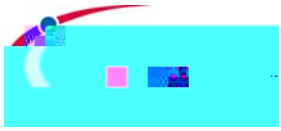


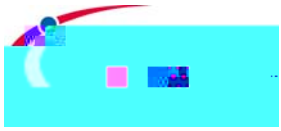


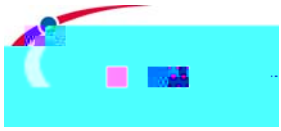
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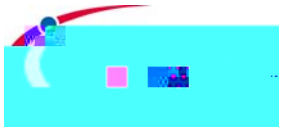


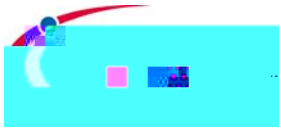












Field ame

S25FL	512	S	AG	M	F	I	0	1	1

Packing type
0 = Tray
1 = Tube
3 = 13” Tape and Reel

Model number (Sector Type)

1 = Uniform 256-kB sectors[54]

Model number (Latency type, Package details, RESET# and V_{IO} support)
0 = EHPLC, SO footprint
2 = EHPLC, 5 × 5 ball BGA footprint
3 = EHPLC, 4 × 6 ball BGA footprint
G = EHPLC, SO footprint with RESET#
R = EHPLC, SO footprint with RESET# and V_{IO}
A = EHPLC, 5 × 5 ball BGA footprint with RESET# and V



